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C-MOS BULK METAL DESIGN HANDBOOK

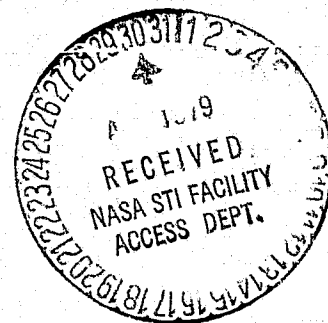
By Teddy M. Edge
Electronics and Control Laboratory

July 1977

NASA

*George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama*

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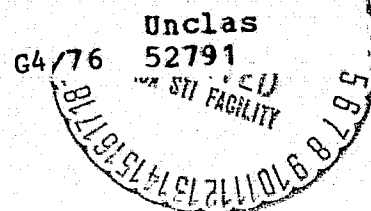


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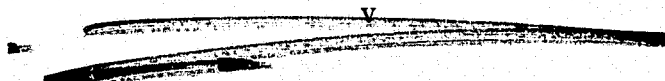
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C-MOS BULK METAL DESIGN HANDBOOK

I. INTRODUCTION

The C-MOS standard cell LSI array design system is a series of computer programs and design automation techniques that automatically translate a partitioned logic diagram into a set of instructions for driving a pattern generator which generates precision mask artwork for complex LSI arrays of C-MOS standard cells.

Two elements are basic to the C-MOS standard cell custom array approach:

1. Standard cell circuit library
2. Computer Aided Design (CAD) programs.

The standard cell concept for producing LSI arrays begins with the design, layout, and validation of a group of custom circuits called standard cells. Once validated, these cells are given identification or pattern numbers and are permanently stored. To use one of these cells in a logic design, the user calls for the desired cell by pattern number. The Place, Route in Two Dimensions (PR2D) computer program is then used to automatically generate the metalization and/or tunnels to interconnect the standard cells into the required function. The computer program accepts the user's input in the form of a properly identified logic net list and produces, as an output, a magnetic tape that will result in the production of a set of instructions for driving a pattern generator. The pattern generator, in turn, generates the seven-level mask artwork necessary to fabricate a C-MOS array.

A. Design System Flow Chart

The system flow chart is shown in Figure 1. Not only are those intrinsic operations that are required to design and produce the LSI arrays included in the flow chart, but other computer programs and design aid techniques are also

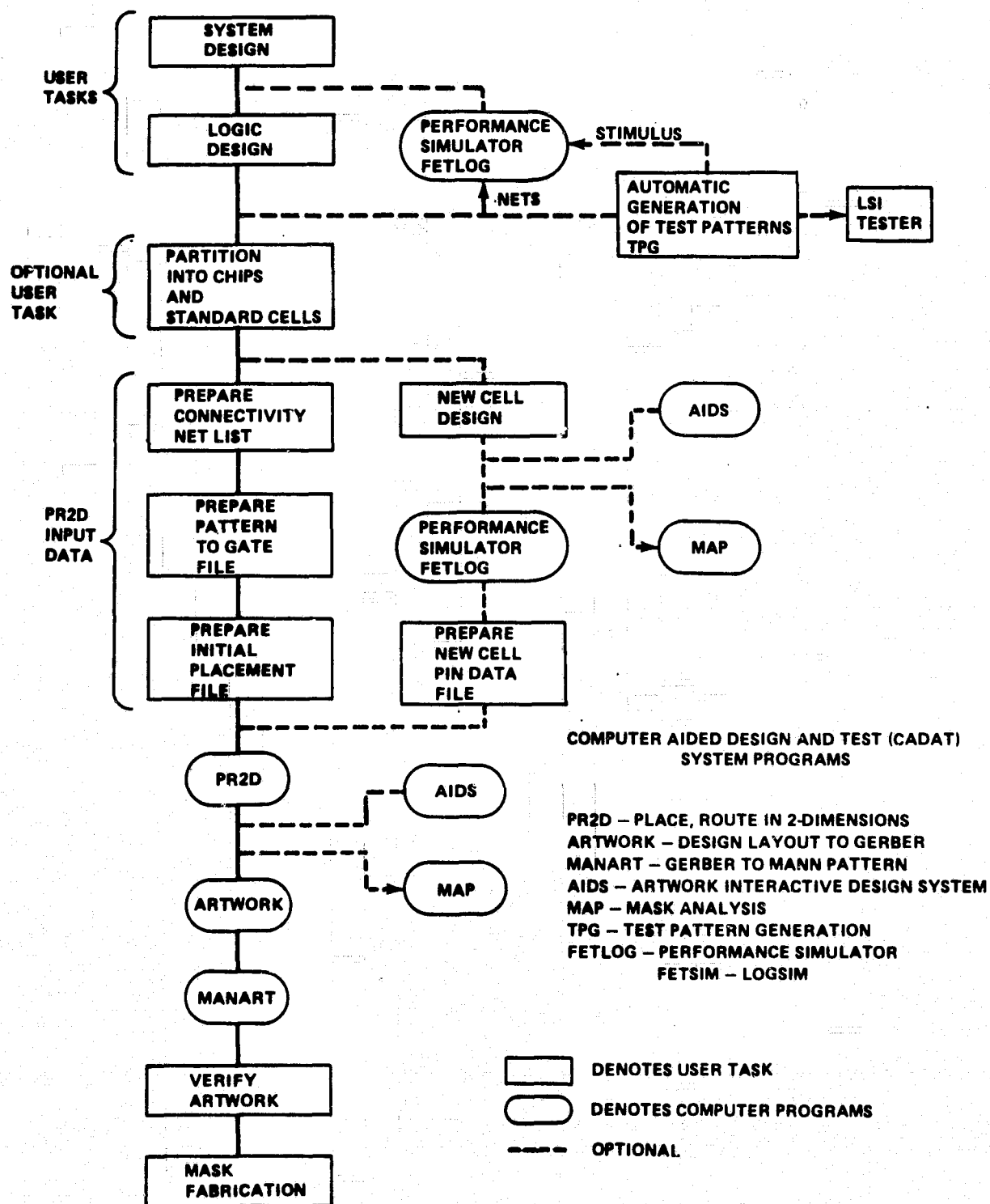


Figure 1. C-MOS standard cell LSI array design system flow chart.

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included whose availability provides the C-MOS LSI design system with flexibility for accommodating a wide range of logic configurations as well as the ability to check and verify the proper operation and performance of the fabricated chip. These auxiliary programs are shown by dotted lines in Figure 1. They include the FETLOG, TPG, and MAP programs.

B. Input Data Requirements

To use this system to produce LSI C-MOS arrays, a user is required to provide, at the minimum, only a logic design that can be partitioned into C-MOS standard cells. The input data requirements for the artwork computer program are derived from the partitioned logic. This input data requirement includes the following steps:

1. The generation of the net list showing the connectivity
2. The sequential numbering of all the logic elements (pattern to gate file)
3. Initial cell placement (may be arbitrary at the beginning).

With the acceptance of these input data, the standard cell LSI array system then provides a low cost quick turnaround capability for generating the mask artwork for the desired complex LSI array.

C. Standard Cell Library

The standard cell library is an open-ended collection of logic circuits implemented with the C-MOS technology. All standard cells have been defined, designed, topologically configured (in accordance with a standard set of C-MOS design rules described in Section III), analyzed, and then permanently stored for future use on magnetic tape. The present library is quite extensive and is designed to meet present and anticipated C-MOS implementation needs. However, it is also open-ended to allow the user to define and design new cells to meet unique future system requirements in the most efficient manner possible.

The C-MOS standard cell data sheets and pictorial representations in Section IV describe the function and performance, along with the artwork, of each of the standard cells in the present family. Each sheet contains the following information:

1. Cell name
2. Cell number
3. Cell width
4. Schematic diagram
5. Logic symbol
6. Logic equation
7. Truth table
8. Capacitance at each cell input and output (if applicable)
9. Delay characteristics versus load capacitance (if applicable)
10. Cell mask artwork.

Section IV also supplements the data sheet information with a brief description of such pertinent items as unique driving capabilities, undefined output states, and influences of output loading on clock rate. A means of estimating intercell wiring capacitance is also given.

The propagation delays and transition times, as documented in this report, were originally generated using the MOS simulation program FETSIM. The device, circuit, and process parameters used in the simulation were based heavily on the parameters determined from measurements on a C-MOS standard cell test chip.

The dynamic data format for each cell varies somewhat as a function of the cell. Generally the area included between the two straight lines that characterize each of the standard cell delays defines the range or spread of delays based on simulated and measured results. Therefore, the propagation delay curves define a range of delays that are expected to occur for each cell. This range in a given cell's stage delay, for a fixed load, can be attributed to the normal variations in the C-MOS process. Such factors as mask alignment, diffusion depths, gate oxide thickness, and doping levels all contribute to the spread of predicted delays. Adding to the predicted spread in the propagation delays for a standard cell are a host of second-order effects that are independent of processing. Included among these are the dependence of propagation delay on

the rise (or fall) time of the driving signal. For multiple-input gates, the propagation delay is also a function of the input to which the driving signal is applied. These effects increase the range over which a cell's propagation delay may occur. They have been implicitly included in the delay curves as given. The delay information was not intended to define the worst case parameters and delays that can exist; however, based on the measured performance of many fabricated and packaged standard cell arrays, the indicated spread in the predicted delays may be considered to be a conservative estimate.

All dynamic propagation information is based on a 10 V supply voltage, an ambient temperature of 25°C, and a 35 ns transition time for the driving signal. Delays are measured between the 50 percent points of the input and output signals.

The primary purpose of the standard cell data sheets and the associated supplementary discussion in Section IV and the user's guidelines in Section II is to provide the logic and system designer with sufficient information concerning each of the standard cells so that he can optimize his selection of the available standard circuits. This should enable the designer to avoid race conditions, optimize critical path delays, avoid excessive loading conditions, and estimate circuit speed, thereby forming the basis for the comparison and evaluation of the cells before the final arrays are processed.

D. System Packaging and Interconnection

One of the principle outstanding characteristics of the C-MOS technology that is used to implement the C-MOS standard cell system is the simplification that it affords in system design and fabrication. A natural result of simplified system design is a more reliable and reproducible design.

Some of the principal characteristics of the C-MOS technology that have direct system design implications are:

1. Only one supply voltage is required.
2. A large operating voltage range (3 to 15 V) may be tolerated.
3. Voltage levels are compatible with other technologies.
4. Output signal levels are firm and virtually equal to system ground and the supply voltage.

5. Quiescent power dissipation per array is in the microwatt range.
6. The noise immunity (static and dynamic) is inherently high.
7. The percentage of noise immunity is virtually independent of the supply voltage.
8. Reliable operation is possible with wide variations in:
 - a. Ambient temperature
 - b. Device processing parameters.
9. There are essentially no dc restrictions on fanout capability.
10. There is a large ratio of transition time to delay time.

The low dissipation, single supply voltage requirements, and high noise immunity as well as the other characteristics provide for gate densities as high as the mask, wafer, and photolithographic technology will permit. This provides the first absolute requirement for significant system performance. However, to achieve this desirable high gate density, the dimensions of the individual transistor geometries cannot be excessive. This places an upper limit on their intrinsic drive capability. The key objective then of the system design should be to develop a package in which the total capacitance of the interconnection media has been minimized. This will provide the optimum system performance. The minimization of capacitance should influence all levels of packaging, from the chip through the final system housing.

1. FIRST LEVEL PACKAGING

Minimum capacitance is achieved by eliminating the first level packaging and mounting the unencapsulated chips directly on some insulating substrate. From a capacitance point of view, wire bonding, solder bumps, flip chips, or beam leads offer similar characteristics. However, the beam lead technology offers many additional advantages; e.g., the ability to simultaneously and reliably bond chips with 40 to 80 pins in a hermetic package, ease of handling, ruggedness, etc.

2. SECOND LEVEL PACKAGING

Consistent with the objective to maximize system performance by minimizing total capacitance, a low impedance second level interconnection media

should be avoided. This means that no ground planes or any other system interconnections that can produce equipotential surfaces should be considered; loose coupled, direct point-to-point wiring above the mounting surface is most desirable.

The interconnection scheme, however, must consider signal crosstalk effects. The evolving of a high impedance interconnection system increases the mutual inductive crosstalk and decreases the capacitive crosstalk. These characteristics are consistent with the C-MOS technology because of its high ratio of transition time to delay time and its high noise immunity. However, because of the low intrinsic input capacitance of the C-MOS devices, there is an upper limit as to the impedance levels that the interconnection media can have before capacitive crosstalk becomes objectionable. This imposes the upper limit on the impedance of the interconnection media. The low limit is primarily determined by operational speed requirements. In general, the low impedance (especially controlled) systems are more costly and less flexible.

II. USER GUIDELINES

A. General Procedure for C-MOS Standard Cell Implementation of Logic Designs

Beginning with system specifications in the form of either logical equations or a logic diagram, groups of logic gates are partitioned (separated) into LSI chips. Then the chip is partitioned by assigning a standard cell to each required function on the logic diagram. (For example, a four-input NAND function will be assigned the standard cell No. 1240.) An example of an LSI array partitioned into standard cells is given in Figure 2. Figure 3 is a graphics checkplot of the array, and Figures 4 through 10 are taken from the final masks. Three basic items are considered during this portion of design:

1. Functional logic and transmission gate guidelines as specified in Section II. F.
2. On-chip and off-chip loading requirements versus the drive capability of each cell.
3. Floating inputs are "tied-off."

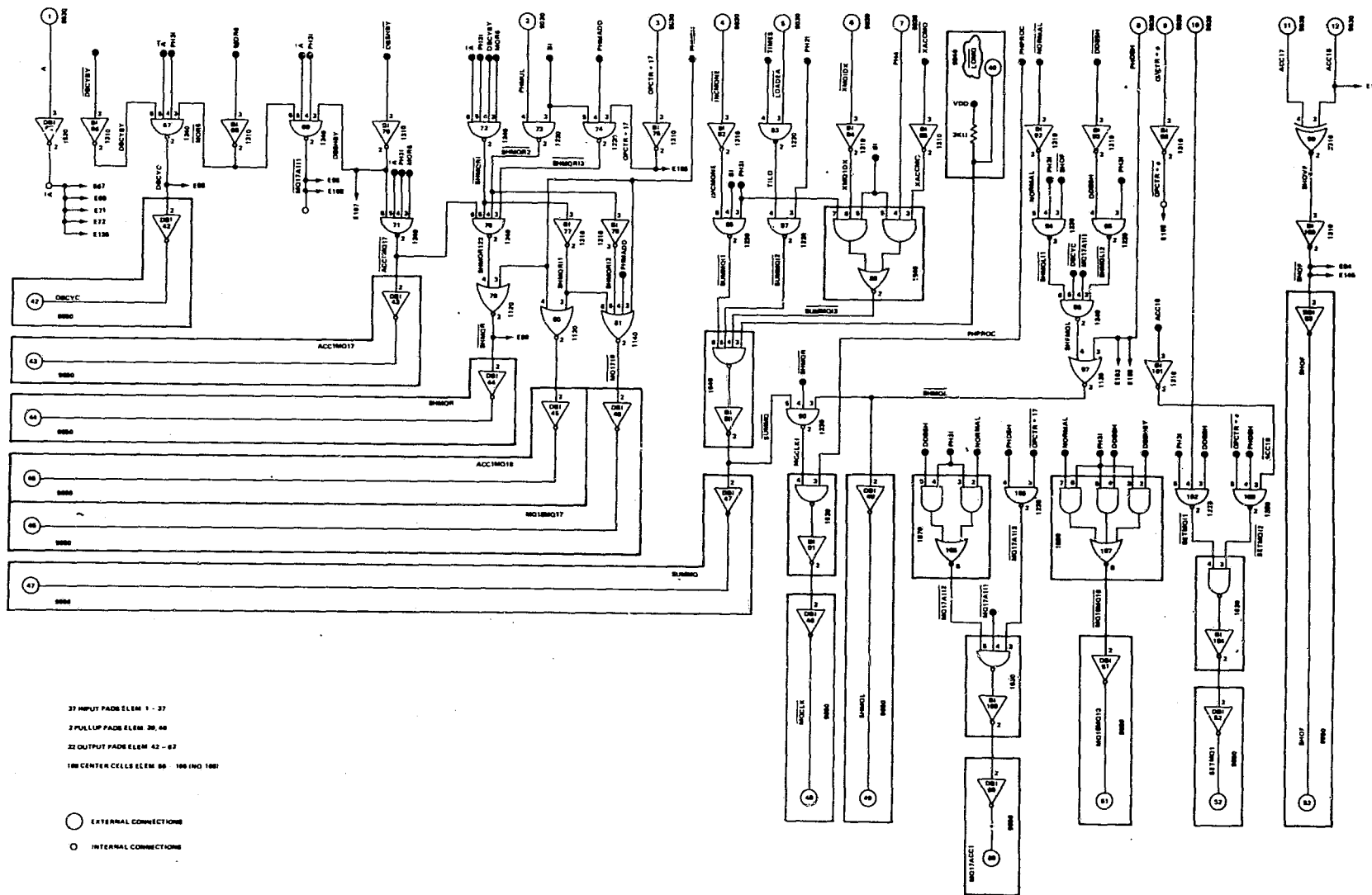


Figure 2. C-MOS data process controller partitioned into standard cells.

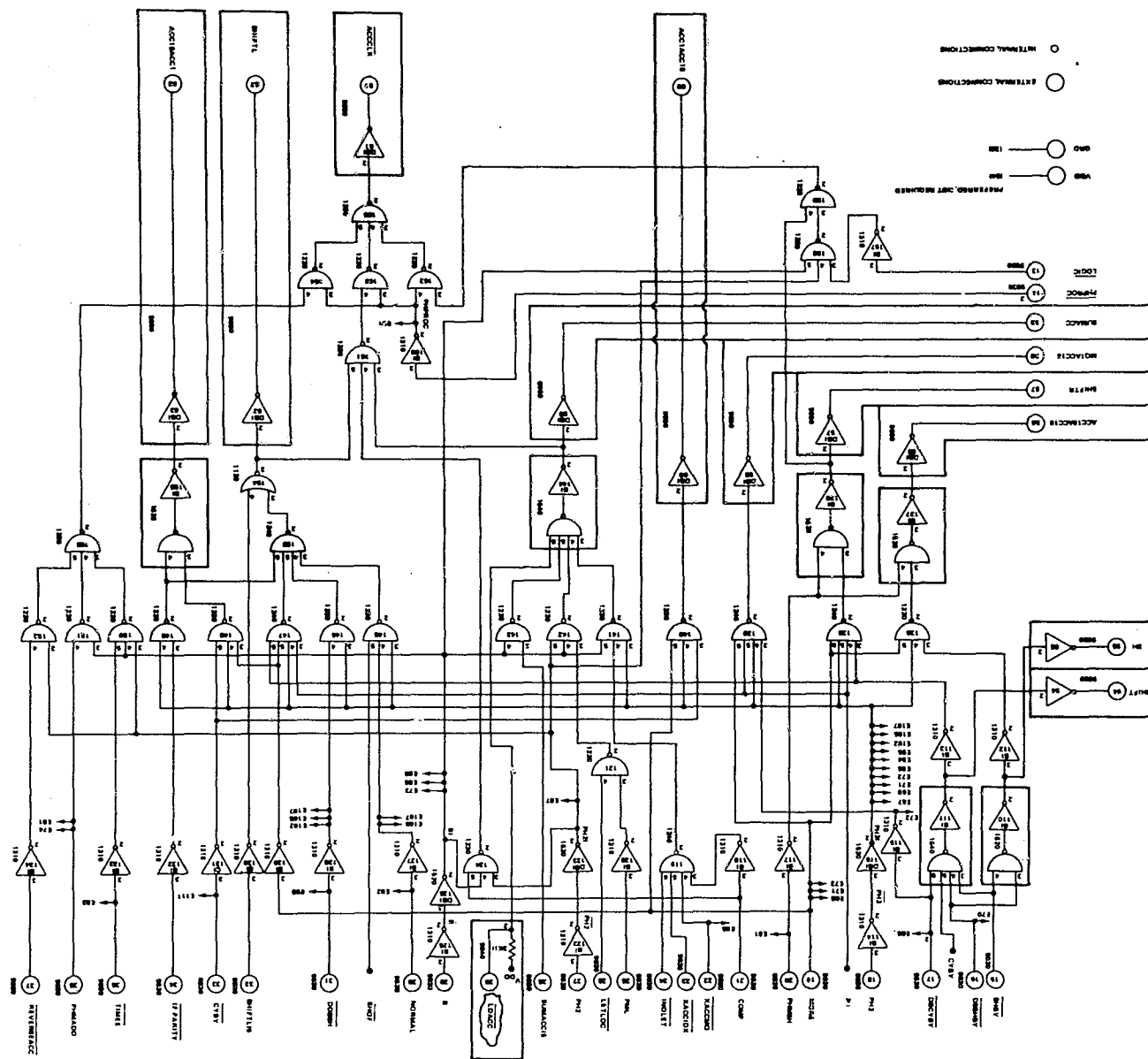


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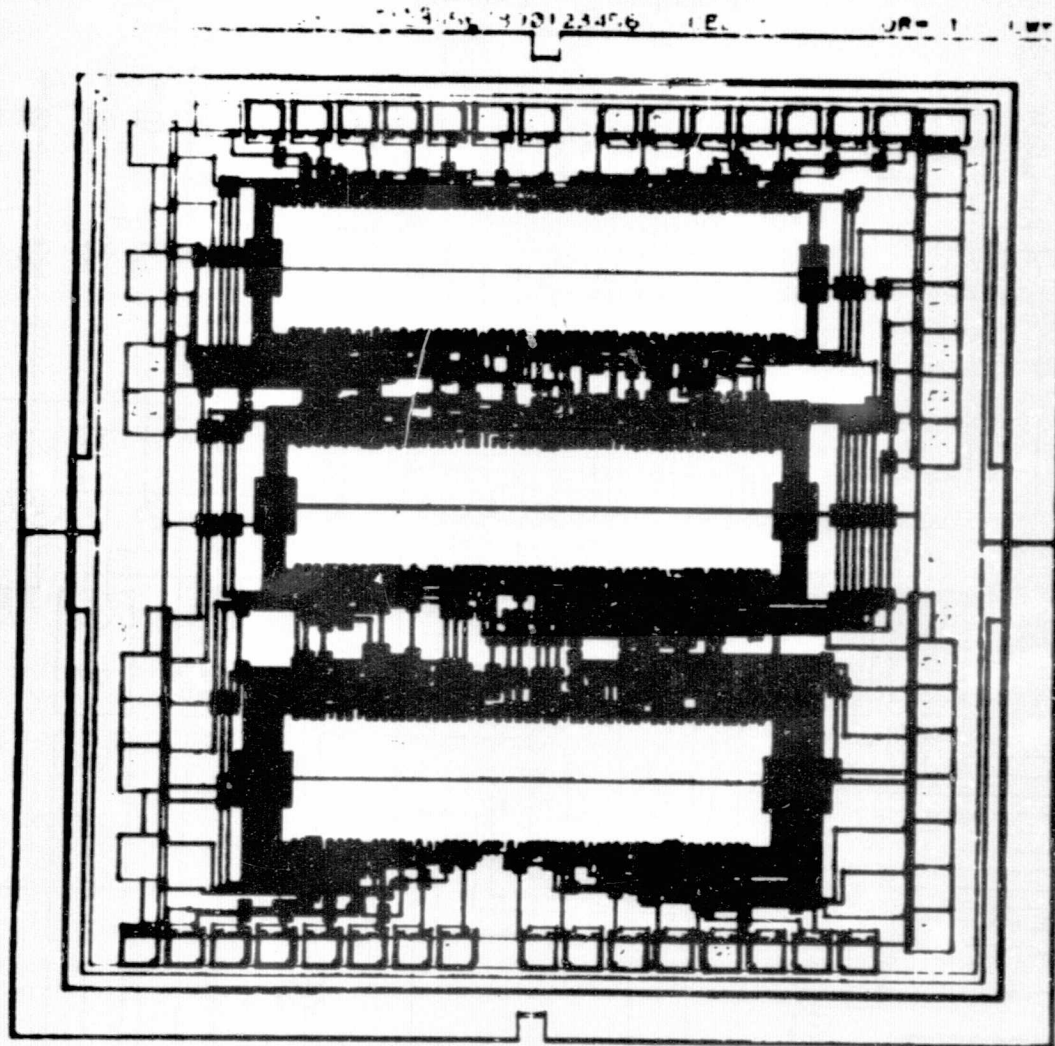


Figure 3. Graphics checkplot of C-MOS data process controller.

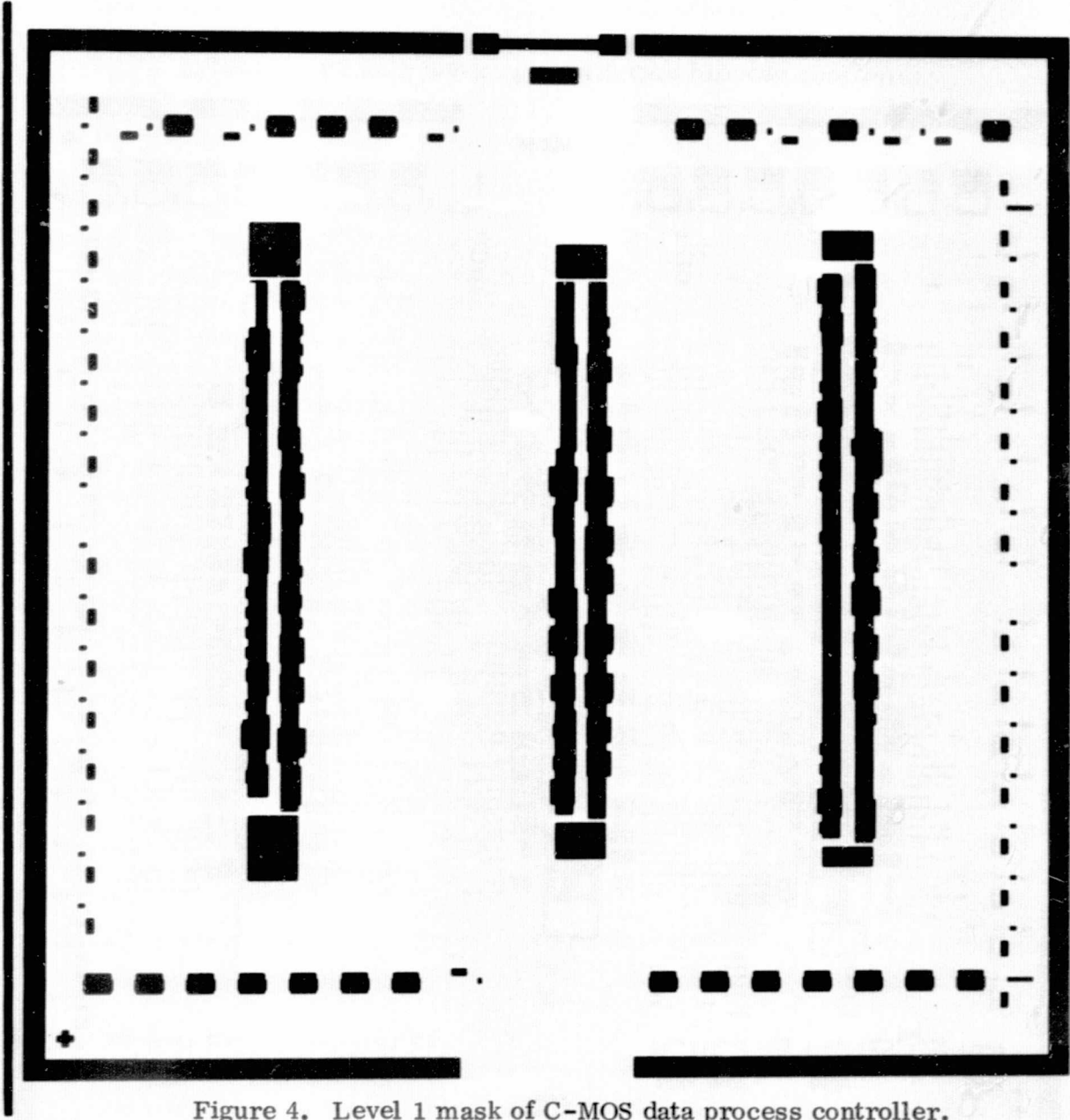


Figure 4. Level 1 mask of C-MOS data process controller.

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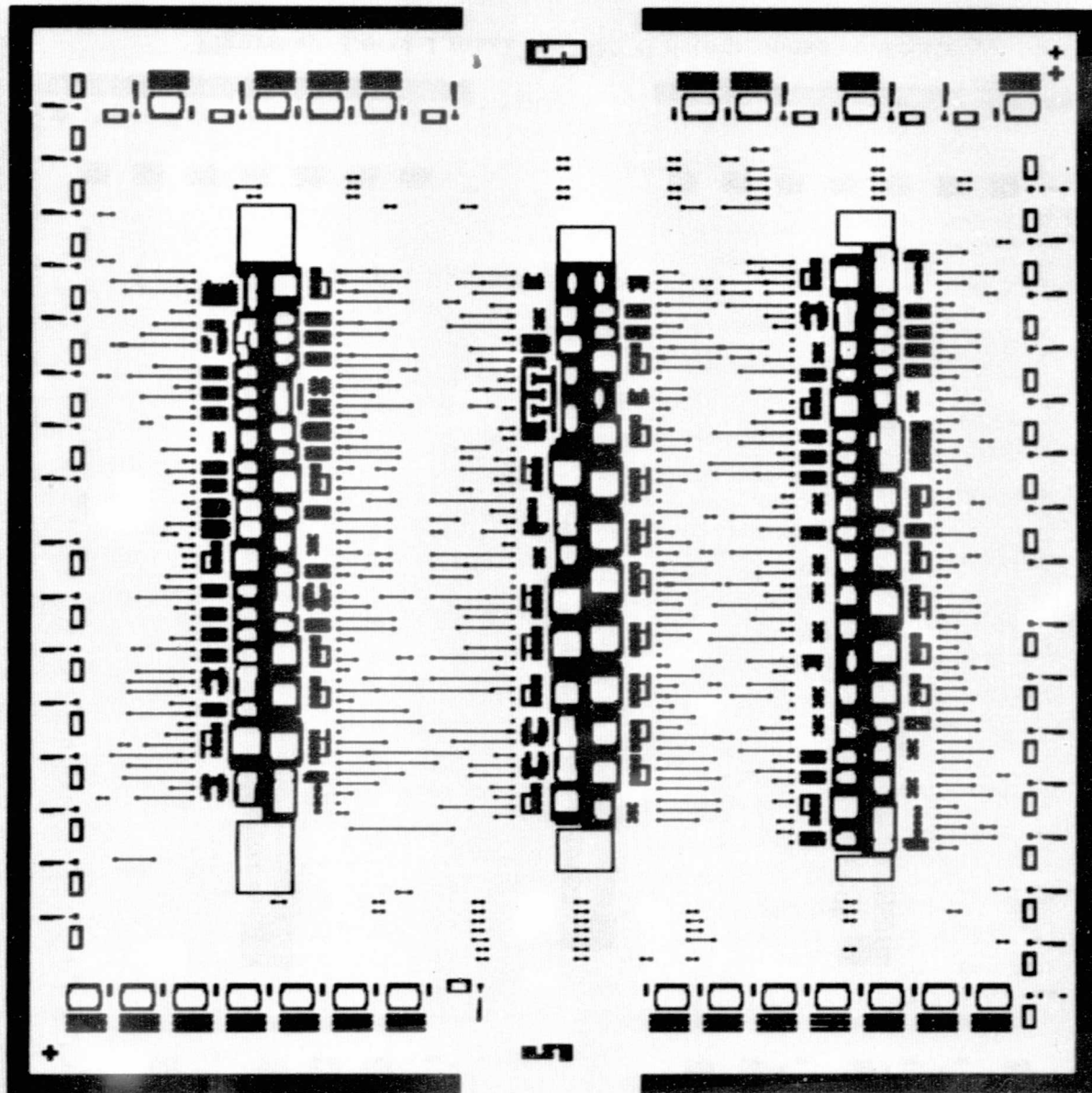


Figure 5. Level 2 mask of C-MOS data process controller.

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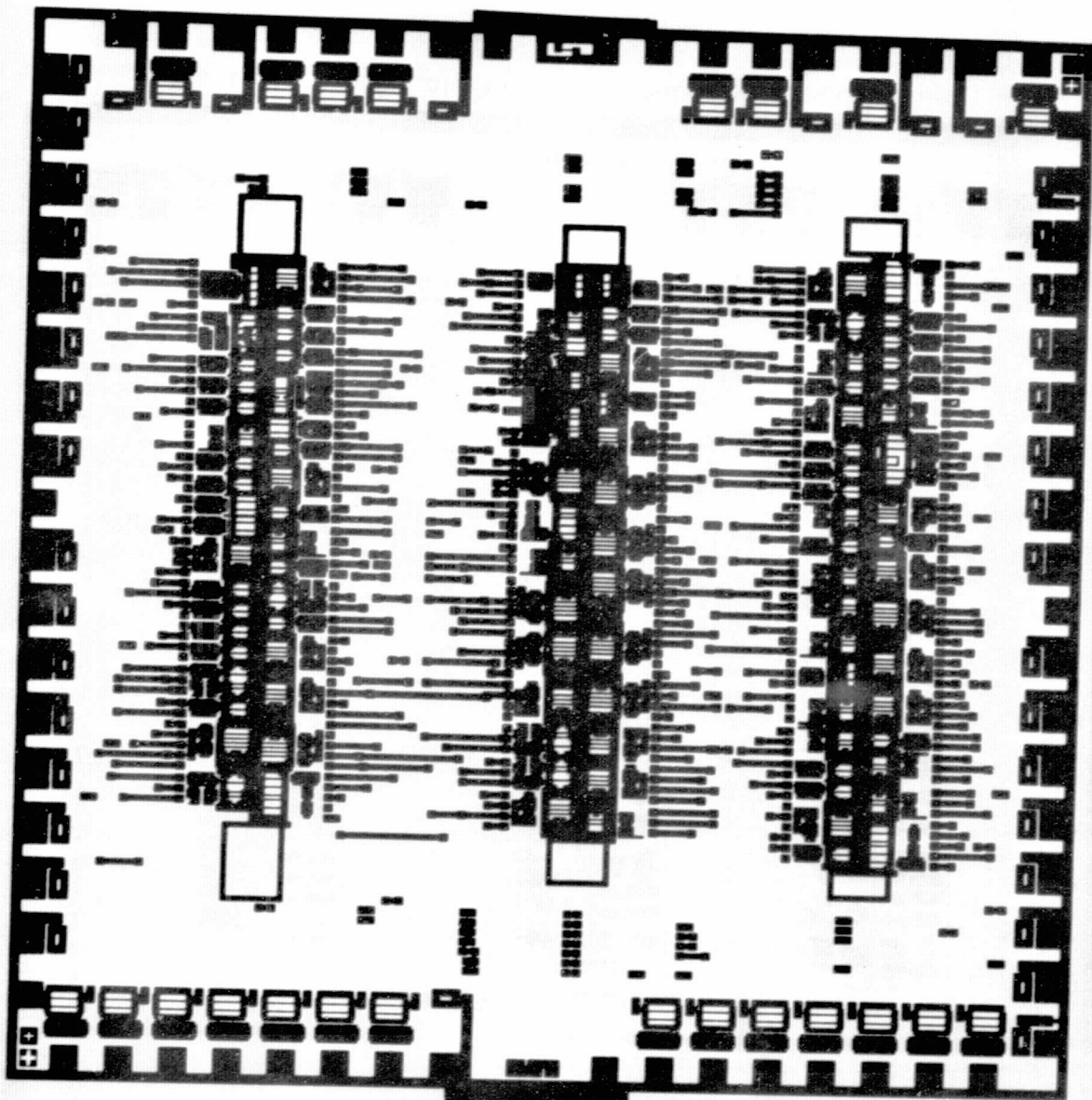


Figure 6. Level 3 mask of C-MOS data process controller.

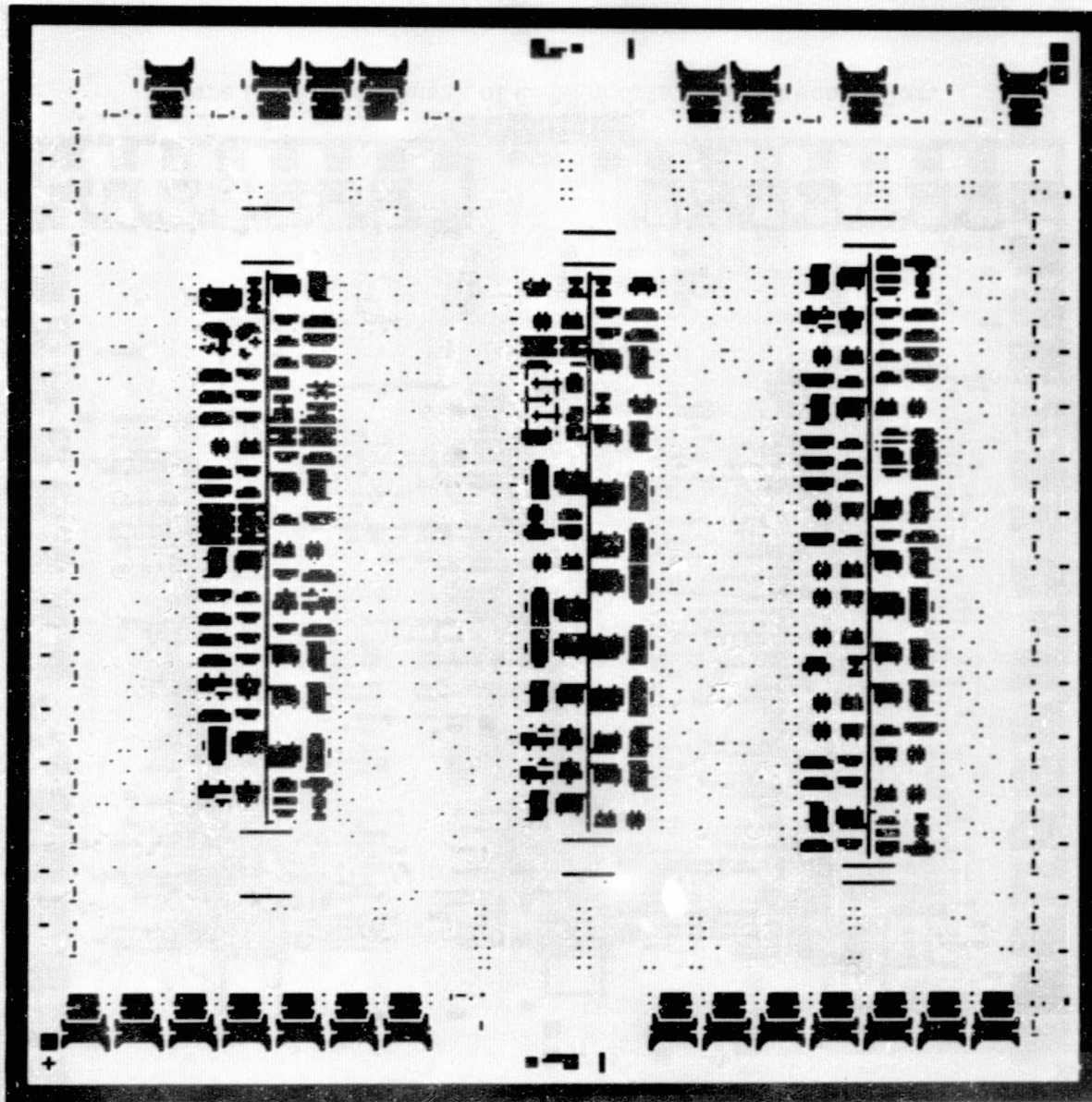


Figure 7. Level 4 mask of C-MOS data process controller.

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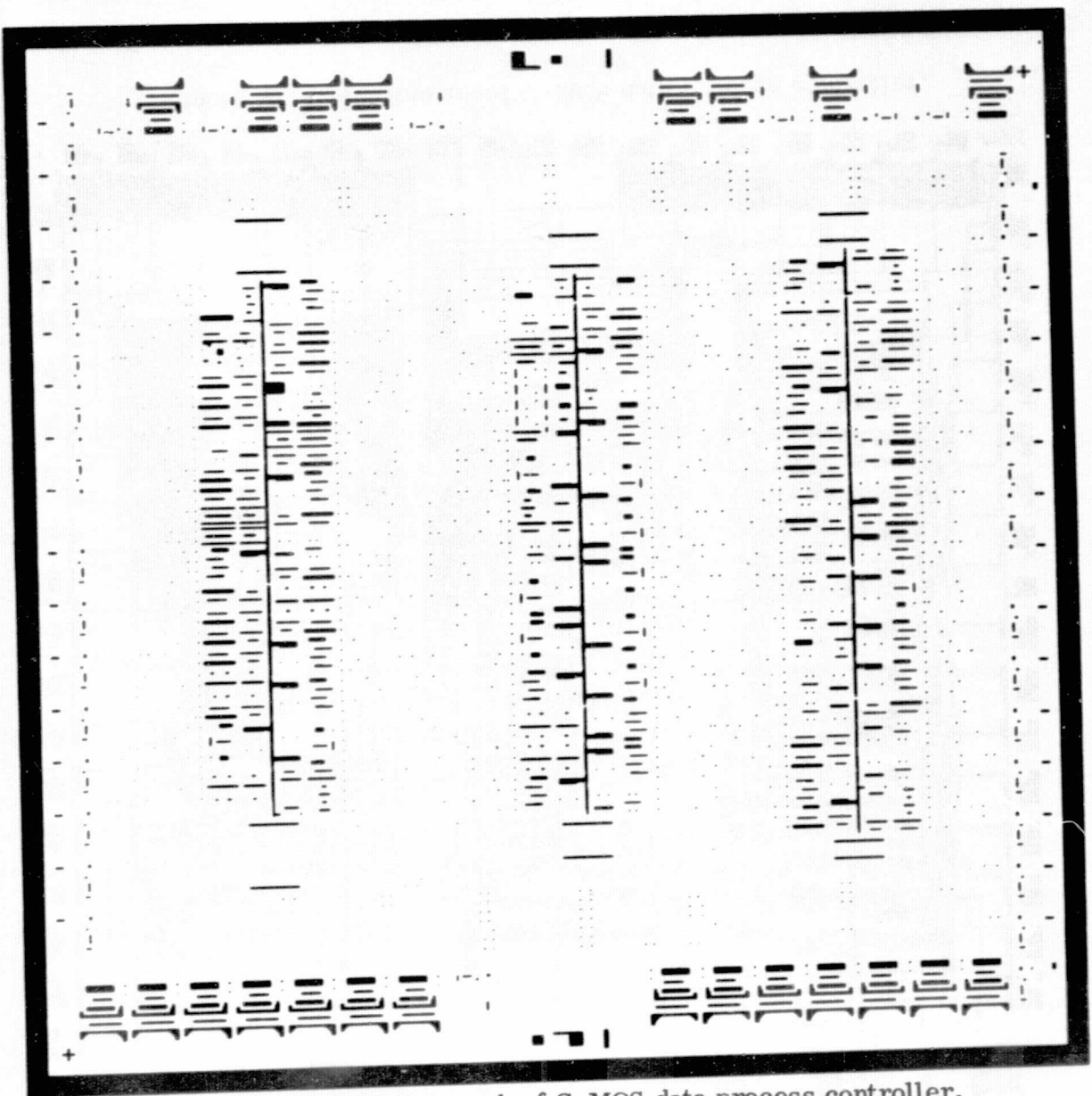


Figure 8. Level 5 mask of C-MOS data process controller.

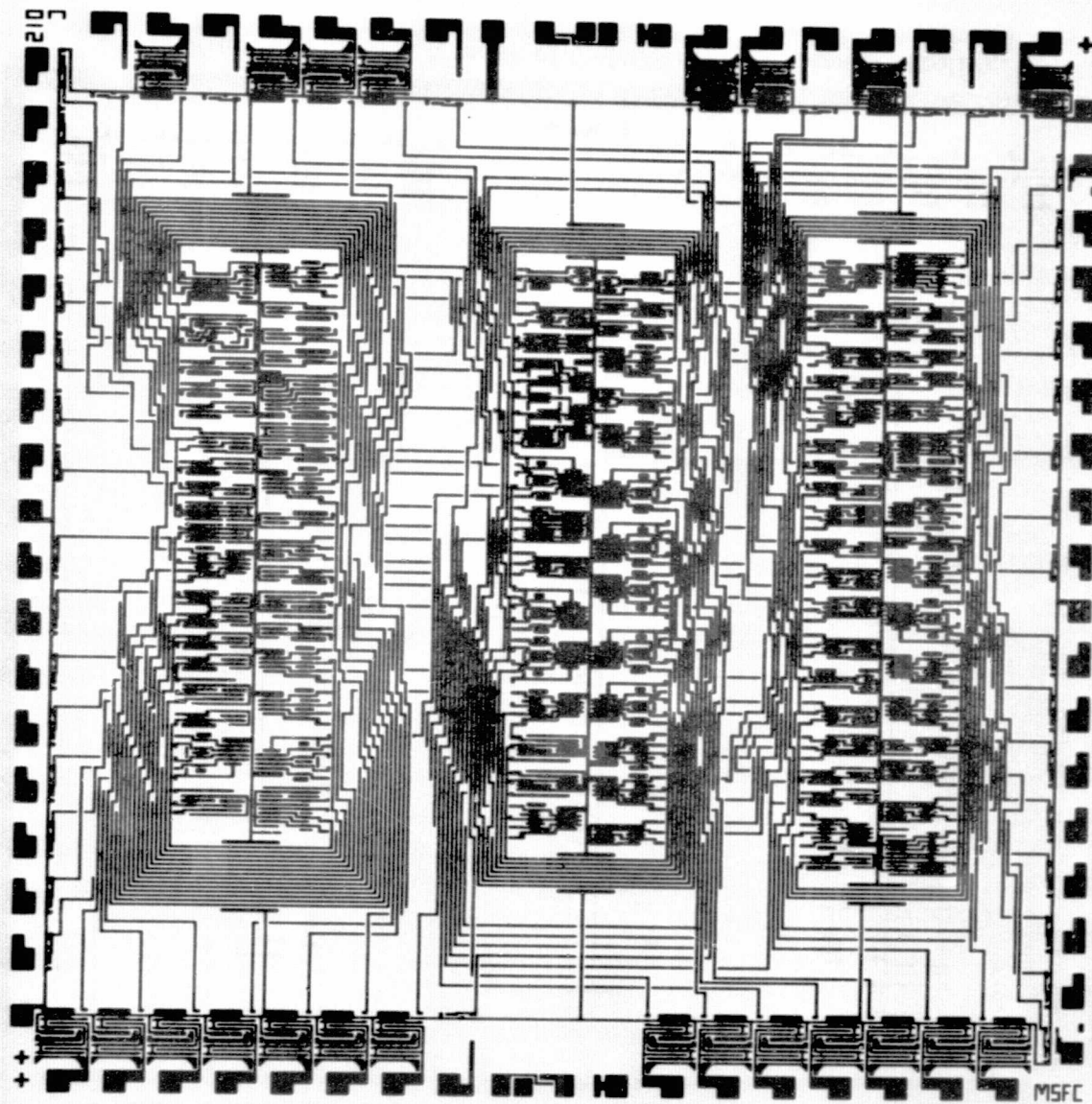


Figure 9. Level 6 mask of C-MOS data process controller.

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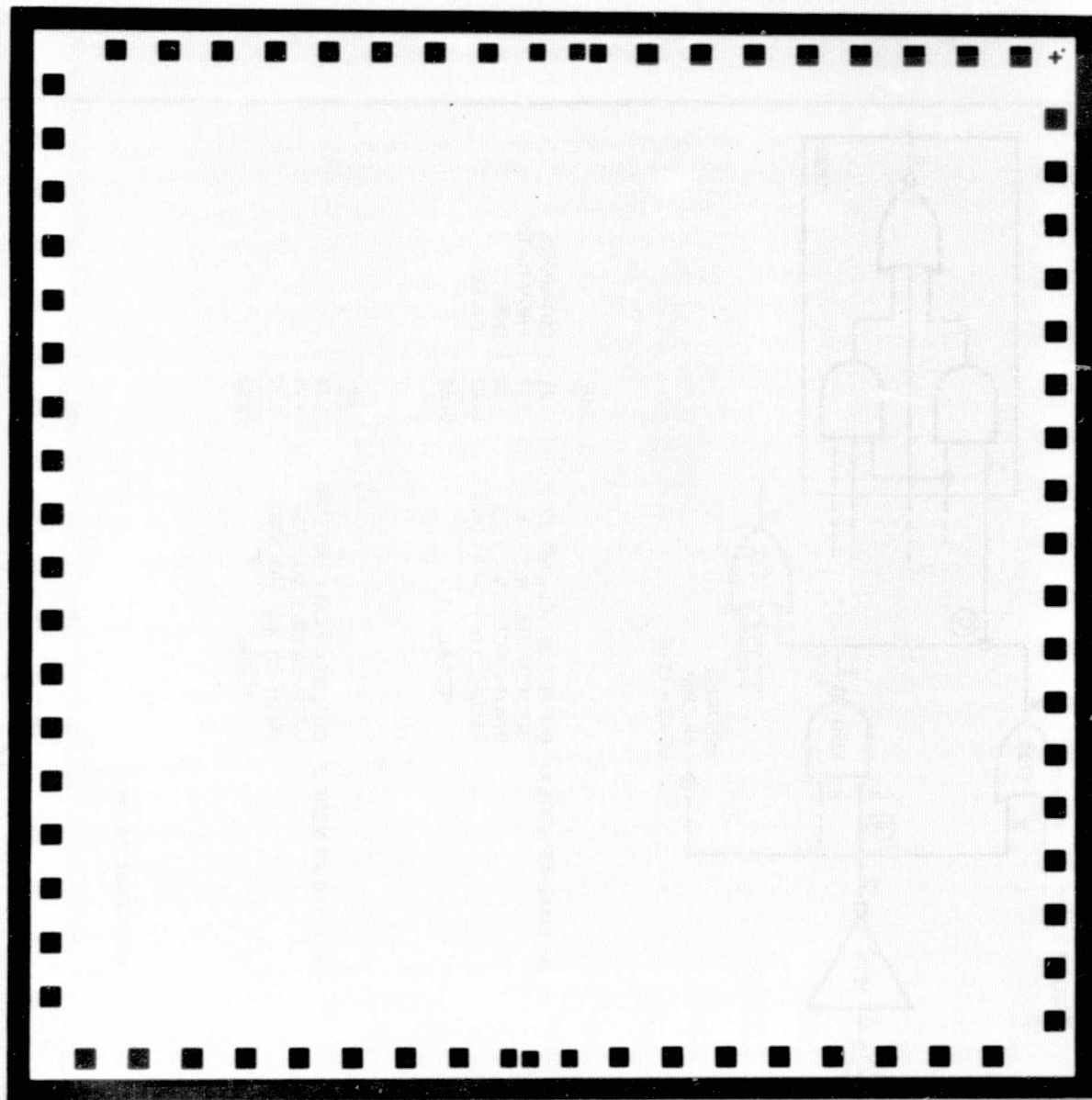


Figure 10. Level 7 mask of C-MOS data process controller.

Before the proposed array is submitted for an initial computer placement run, critical signal paths should be found and examined. The delay characteristics as specified on the data sheet of each cell are used to locate and evaluate possible race conditions. An example illustrating the use of these characteristics is presented in Figure 11 and discussed in Section II. B.

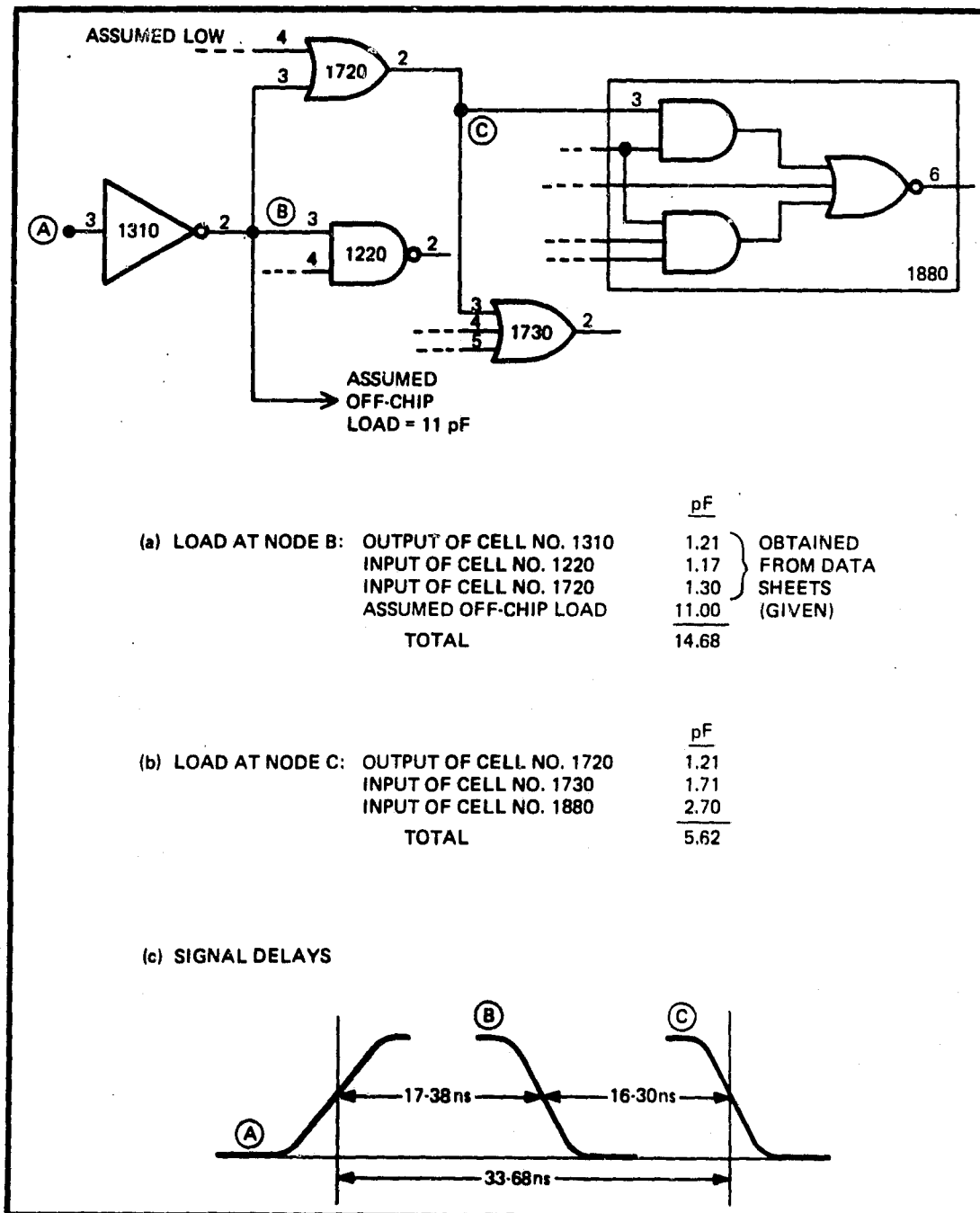


Figure 11. Example illustrating delay calculations.

After an initial computer placement run is made, the metalization and tunnel lengths associated with the intercell connections in the critical paths may be estimated and used in reevaluating the critical path delays previously estimated. The appropriate tunnel and metalization lengths can be obtained from a graphics checkplot of the proposed cell placements. Two additional considerations enter at this time:

1. Metalization and tunnel loading capacitance (Section II. C)
2. Resistive effects of tunnels (Section II. D).

B. Delay Characteristics

After partitioning the logic into the selected standard cells and the net list generated, analyses can be made of the critical path delays, race conditions, and loading conditions. This begins by calculating the total capacitance associated with each node of the signal path. The total capacitance is defined as the sum of the input capacitance of all gates connected to this node and the output capacitance of the driven circuit. (Both the input capacitance and output capacitance for each circuit may be obtained directly from the data sheets.) However, if the cell is driving an off-chip load, then this load must also be included. The example in Figure 11 aids in illustrating this procedure.

By referring to the data sheet for the buffer inverter cell (1310), Figure 12, and using the calculated load of 14.7 pF, the stage delay (node A to node B) can be estimated to be between 17 and 38 ns. The variance in the estimated stage delay for the 1310 cell is due primarily to the tolerance range of the C-MOS processing parameters. Similarly, by referring to the data sheet for the two-input OR gate (1720), Figure 13, and using the calculated load of 5.6 pF, the stage delay (node B to node C) can be estimated to be between 16 and 30 ns. If all the cells shown are located on one chip, a uniform set of processing parameters can be assumed. This permits accurate estimates concerning the relative delays associated with different logical paths on the same chip.

C. Metalization and Tunnel Capacitance

The effects of the loading capacitance associated with the intercell wiring and/or tunnel interconnections should be accounted for under either of the following conditions:

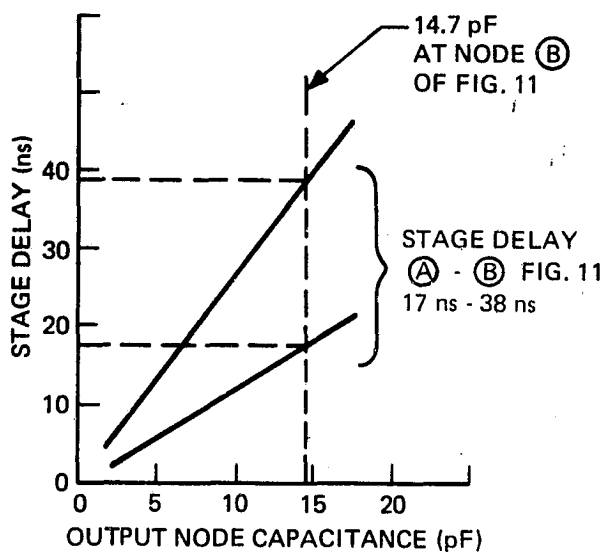
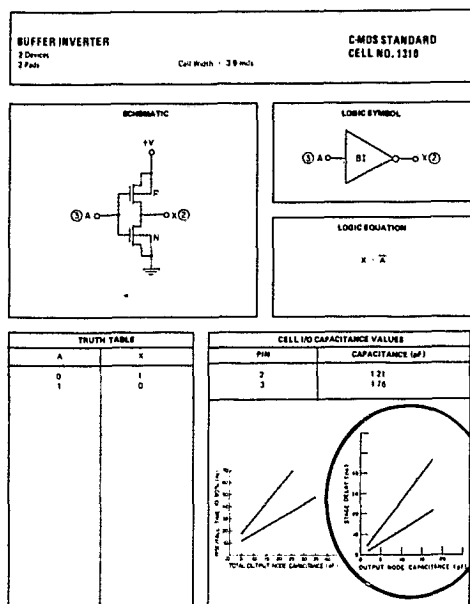


Figure 12. Delay calculations using stage delay, output node capacitance curves of the data sheet for cell No. 1310.

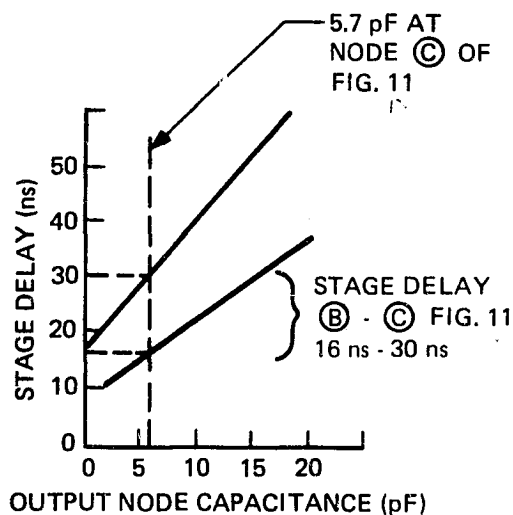
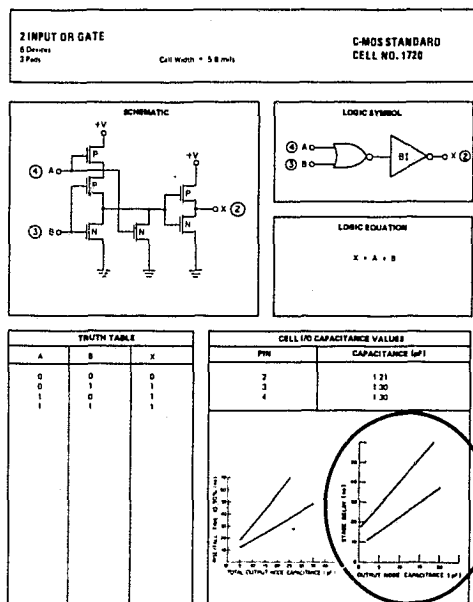


Figure 13. Delay calculations using stage delay, output node capacitance curves of the data sheet for cell No. 1720.

1. The length of metal connected to a single node exceeds 200 mils.
2. The length of tunnels connected to a single node exceeds 20 mils.

(The length of the tunnel and/or metalization may be obtained from a graphics checkplot of the mask artwork, such as shown in Figure 3.)

For these conditions, the capacitive loading associated with either the metalization or the tunnels can be estimated by:

$$C_{\text{METAL}} = (0.008 \text{ pF}) \times (\text{length of the metal in mils})$$

$$C_{\text{TUNNEL}} = (0.08 \text{ pF}) \times (\text{length of the tunnel in mils})$$

Therefore, the total capacitive load is the sum of the metalization and tunnel capacitance, the cell input and output capacitance, and the off-chip capacitance load,

$$C_{\text{LOAD}} = C_{\text{CELL OUTPUT}} + C_{\text{CELL INPUTS}} + C_{\text{METAL}} \\ + C_{\text{TUNNEL}} + C_{\text{OFF-CHIP}}$$

D. Resistive Effects of Tunnels

In addition to the effective loading capacitance associated with the inter-cell P+ tunnel connections, it may be necessary to consider the RC delays introduced by the resistive nature of the tunnels. This effect is most significant when a buffering circuit, such as cell No. 1520, is used to drive a heavy off-chip capacitive load through a long tunnel. The point at which the RC delay, introduced by a tunnel, may no longer be neglected is generally a function of the driving circuit.

Assume that the RC delay may generally be neglected for any of the following two conditions:

1. The driving circuit is cell No. 1520 and the interconnecting tunnel length is less than 5 mils.

2. The driving circuit is cell No. 1310 and the interconnecting tunnel length is less than 10 mils.

For those cases where the interconnecting tunnel is too long to neglect, the resistance of the tunnel may be approximated by

$$R_{\text{TUNNEL}} = (83 \text{ ohms}) \times (\text{length of the tunnel in mils}).^1$$

Figure 14 illustrates delay calculations that take into account the resistive effects of a tunnel.

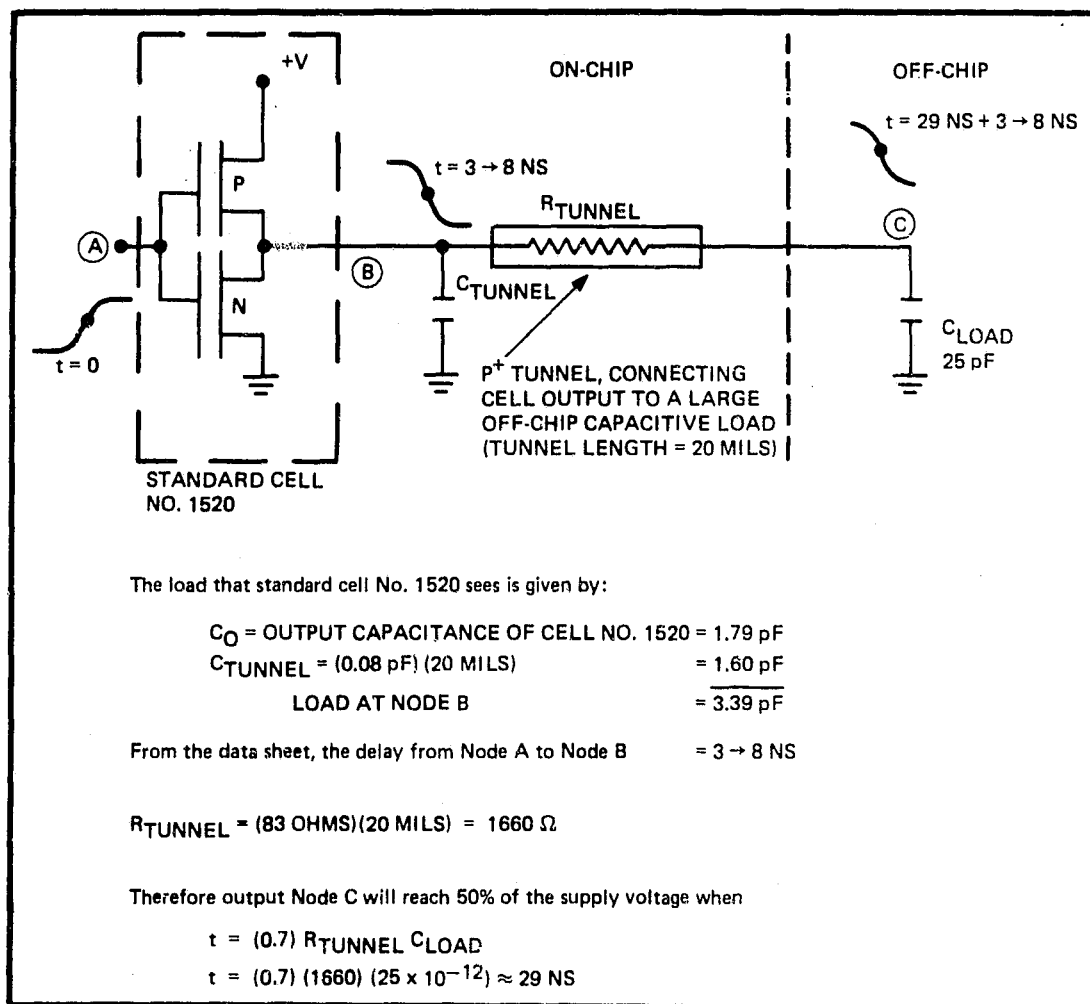


Figure 14. Example illustrating calculations of signal delay considering tunnel resistive and capacitive effects.

1. The length of the tunnel may be obtained from a graphics checkplot of the mask artwork of the LSI array.

E. Off-Chip Loading

An illustration of the off-chip capacitance is shown in the following tabulation for a system using ceramic dual-in-line packages.

<u>Type of Off-Chip Load</u>	<u>Value</u>
Each ceramic in-line package (24 pin)	3.5 pF
Each ceramic in-line package (40 pin)	5.5 pF
Each socket terminal	1.0 pF
All interchip (point to point with no ground plane) wiring	0.7 to 1.7 pF/in.
Each input/output board pin ²	3.0 pF
Each input/output board pin socket	5.0 pF

From the preceding values it is seen that in addition to interchip wiring capacitance and on-chip loading capacitance, an additional 5.5 pF (or 3.5 pF) must be included each time the signal goes on or off a chip.

F. Transmission Gates and Functional Logic

The C-MOS standard cell family is made up of circuits designed using either a functional logic (FL) and/or a transmission gate (TG) relay logic approach. Each method has its unique characteristics and advantages, some of which are as follows:

1. Standard Cells Implemented with Functional Logic

- a. The outputs of functional logic cells may not be tied together (the wired OR).
- b. Each circuit provides, virtually, electrical isolation between output and input nodes — a noise immunity approximately equal to 40 percent of the supply voltage.
- c. Each circuit amplifies the input waveform and may therefore be used to reshape the signal waveform.

-
2. This measurement pertains to an 80 pin, 0.0625 in. thick commercially available board.

- d. The inherent nature of functional C-MOS logic is to provide one signal inversion for each stage of circuitry. Therefore, when a cell implemented with functional logic supplies the AND function, it must contain at least two levels of circuitry; the invert or NAND function requires one level of circuitry.

2. Standard Cells Implemented with Transmission Gate Logic

- a. The outputs of transmission gate cells may be tied together provided that no two transmission devices with outputs connected are placed in the conducting state at the same time.
- b. Transmission gate logic does not provide signal amplification. Therefore, when cascading several such devices, a functional logic circuit may be placed between them. This suggestion is based primarily on the need to maintain sharp waveforms and fast stage delays. It is not necessary or required to ensure proper operating levels.
- c. In contrast to functional logic, transmission gate logic provides noninversion functions.

G. Drive Capability

The standard cell family can be divided into four groups of circuits, with members of each group having essentially the same dynamic and/or static drive capability; that is, standard cells in the same group will have approximately the same output rise or fall times for the same load.

- o Group I cells are characterized by those circuits implemented with transmission gate logic. Cells in this group have no drive capability of their own. Each cell may be considered to be a relay circuit that has a finite conducting resistance and an infinite "off" resistance.
- o Group II cells are characterized by output circuitry implemented with standard size nonbuffered transistors. This group comprises the bulk of the standard cell family. Generally these cells should be used when their total output load is less than 8 pF. Otherwise they should be followed with a buffering circuit.

- o Group III cells feature output transistors roughly three times as large (powerful) as those of group II. These cells should be used when their total output load is less than 25 pF but greater than 8 pF.
- o Group IV presently encompasses two cells. These cells serve as buffers for all loads greater than 25 pF.

As a guide to the user, each cell's drive capability is listed on the data sheet. TG indicates that the cell is in group I, BI indicates that the cell is in group III, DBI indicates that the cell is in group IV, and the absence of any of these three symbols indicates that the cell is in group II.

H. Floating Inputs

All inputs should be connected either to the output of another gate or to one of the low impedance signal levels. A floating input can result in improperly functioning gates.

III. SPECIFIC C-MOS DESIGN RULES

A. Components

C-MOS circuits are normally made on an N-type substrate; therefore, a P-type well is required for N-channel devices. This well must be connected to the lowest potential of the device(s) in the well. If additional N-channel devices are to be operated at higher potential, separate wells are required.

All MOS transistors will be enhancement units; transconductance will be directly proportional to mobility (μ) and channel width (W), and inversely proportional to channel length (L). Length and width are restricted by process and photographic limitations to 0.3 mil minimum length and 0.7 mil minimum width. Since the N-channel units have higher mobility, they will have approximately two times the transconductance of identical geometry P-channel units; therefore, for matching transconductance, the P-channel units (with both N-channel and P-channel using the minimum 0.3 mil length) will require approximately two times the width of N-channel units.

Tunnels may be utilized where metal crossovers are necessary; however, circuit layout should be such that the number of tunnels is minimized because of the added area and impedance they entail. Tunnels may be either P+ or N+ diffusions and may be an extension of the device source or drain. P+ tunnel sheet resistance will be approximately 60 ohms per square, and N+ tunnel sheet resistance will be approximately 10 ohms per square.

B. Input Gate Protection

The protective diode circuit shown in Figure 15 should be utilized in all high impedance gate inputs leading to external terminals. Diodes serve to protect the device against burnout resulting from accumulation of static charge on package terminals.

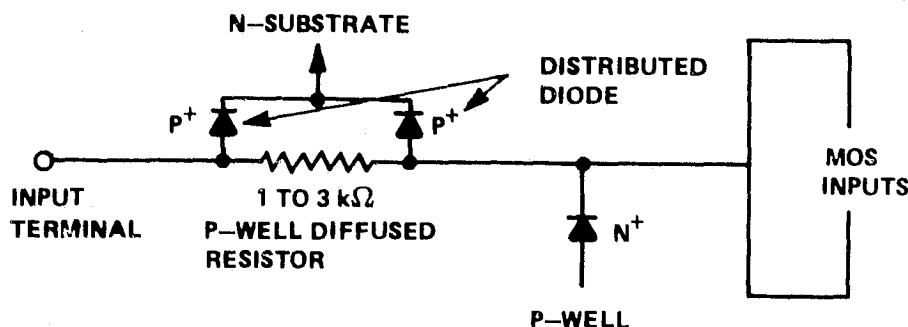
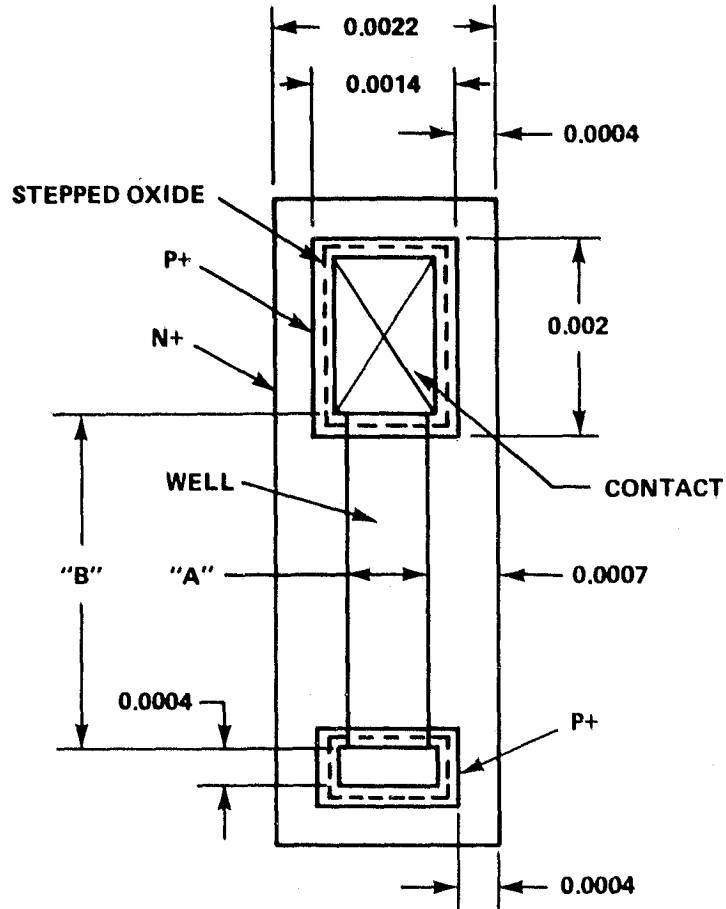


Figure 15. Protective diode circuit.

The 1 to 3 kΩ protective resistor is achieved by the well diffusion and is shown in Figure 15. N+ guard bands are necessary to surround it. The protective diodes are formed by a P+ diffusion into both ends of the resistor diffusion.

The table in Figure 16 outlines various combinations of well diffusion length and width to obtain this resistance. The dimensions are based on 750 ohms per square well diffusion, taking into account side diffusion. The area of the P+ diode at the pad end of the resistor is fixed at 2.8 mils², and the P+ area of the diode in the well is 1.3 mils² minimum, but should be made larger where space permits to sharpen the forward diode characteristic.



WELL DIM'S	
"A"	"B"
0.0005	0.0023
0.0006	0.0027
0.0007	0.0031
0.0008	0.0034
0.0009	0.0038
0.0010	0.0042

SCALE: 500X

Figure 16. Protective 1 to 3 k Ω resistors.

C. Guard Bands

Protective guard bands must surround each separate MOS device, tunnel, well, and diode or surround combinations of MOS devices that are interconnected through common diffused regions. These guard bands serve to prevent leakage and generation of spurious MOS devices. The guard band for the well is a P+ diffusion that has an inside boundary line-to-line with the well periphery and must extend at least 0.6 mil outside the well to allow for side diffusion of the well junction. The well guard band should continue inside the well also to serve as a guard band for N-channel devices and N+ diodes. This guard band may also serve as a tunnel for the ground pad to each N-channel transistor with a source-to-ground connection. Contact to the well may be made to any part of this continuous P+ well guard band. P-channel devices, tunnels, and P+ diodes must be surrounded by N+ guard bands. Contact to the substrate may be made through this continuous N+ guard band which may also be utilized as a tunnel to provide V_{DD} supply voltage to each P-channel transistor with a source-to- V_{DD} connection. Guard bands may be narrow stripes (0.4 mil minimum), or they can be large diffused areas. Guard bands are also used to ensure positive device cut-off. Cutoff is accomplished by having the gate metal, as it leaves the end of the channel, cross a guard band prior to reaching the stepped oxide.

On all circuits, space should be allotted for the inclusion of separate N- and P-channel test transistors.

D. Layout Drafting

If the layout is to be done manually, all drawings should be made at 500X, using paper having a 10 line per inch grid. Thus, each line represents 0.2 mil, and a line midway between two grid lines represents 0.1 mil, which is the smallest acceptable dimension. Dimensions are not required on the drawing; however, scale 2 mil (1 in.) marks should be labeled on an X-Y reference axis, as shown in Figure 17. If the layout is to be done using computer graphics, a similar grid scale should be selected.

E. Layout Geometries

Since there is an inverse relationship between C-MOS circuit probe yield and chip size, layout technique is a significant factor in determining both. The layout designer is advised to study the schematic or logic diagram and break it

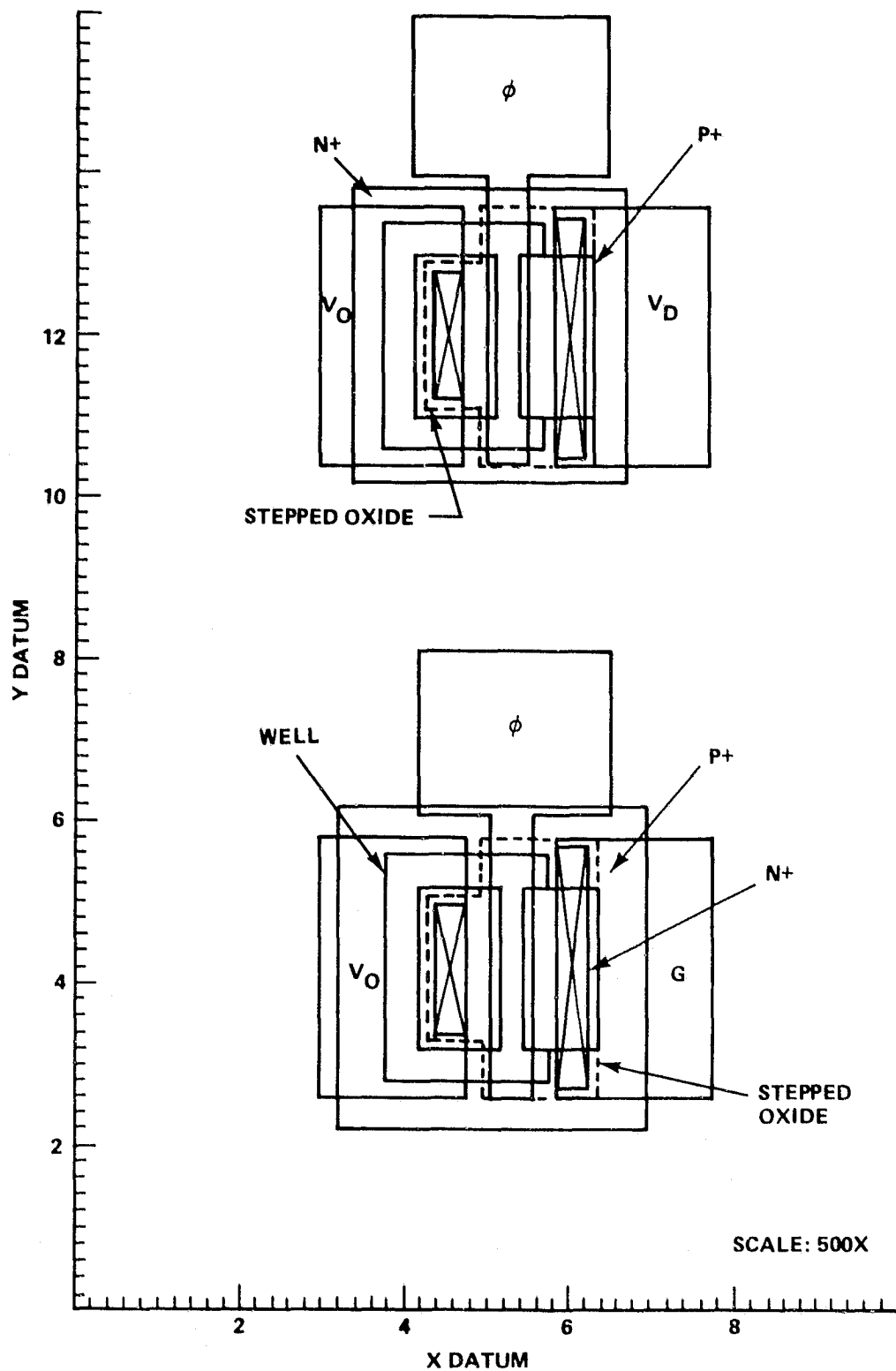


Figure 17. P- and N-channel MOS test devices.

up into cells. Since most digital circuits consist of repeatable cells (i.e., counters, registers, adders, decoders, etc.), early effort should be spent on getting the most compact cell design with easy inputs and outputs. Within a cell, the designer should look for common source-drain points between adjacent transistors. These may be joined together in the layout as a single diffused region without the necessity of running a guard band between them. In this manner it is possible to lay out more complete cells in a series string of common diffusion without any guard band interruptions between the component transistors.

The normal layout procedure is to lay the cells out in the X-direction with the channel lengths in that direction and the channel widths in the Y-direction. In addition, the complementary P- and N-channel transistors are aligned directly above and below each other in the N-substrate and P-well, respectively, with metal interconnects for the gates and diffused regions running between them. Clocks, resets, set lines, etc., are normally drawn in the X-direction feeding into the cells where applicable.

To conserve space and limit the number of wells, N-channel devices of one cell, or stage, are normally placed back-to-back (Y-direction) with the N-channel devices of some other cell, or stage. The spacing between these adjacent N-channel devices is usually dictated by the number of horizontal metal interconnects of each cell. A typical C-MOS layout, therefore, consists of alternate double rows of back-to-back N-channel and back-to-back P-channel devices.

If the P+ guard band of the well is to be used as a tunnel for the ground supply (normal practice for C-MOS circuits), large area contacts should be made at opposite ends of each well and connected directly to the ground pad without any other tunnels along the way. Particular care should be taken on the relative placements of these ground contacts and output transistors of large width to minimize the resistance between them.

F. Layout Design Rules

This discussion details design rules and tolerance specifications for specific items such as transistors, metal interconnects, bond pads, alignment keys, etc. In most instances, a minimum dimension is specified, either for the width of a line or a clearance value. It should be emphasized that these values are minimum values and should be increased wherever space permits. In addition, pattern runout, i.e., the variation in dimensions as one scans

across a succession of repeated patterns, will be minimized if the layout is such that critical dimensions and clearances are aligned in one direction only with relaxed values along the other axis. This is true not only in the process of mask fabrication, wherein the step-and-repeat process is utilized to duplicate patterns, but also in wafer alignment, wherein operator judgment during mask-to-wafer alignment is the critical factor.

1. DEVICE DESIGN

Figure 18 illustrates a typical N-channel device located in a well and a corresponding P-channel device located adjacent to it in the substrate. Section A-A of Figure 18 indicates the relative position of diffusions, contact openings, and metal. Seven masks are required to make these complementary circuits. In process sequence, they are the well, P+, N+, stepped oxide, contact, metal, and passivation. The first six are indicated in Figure 18.

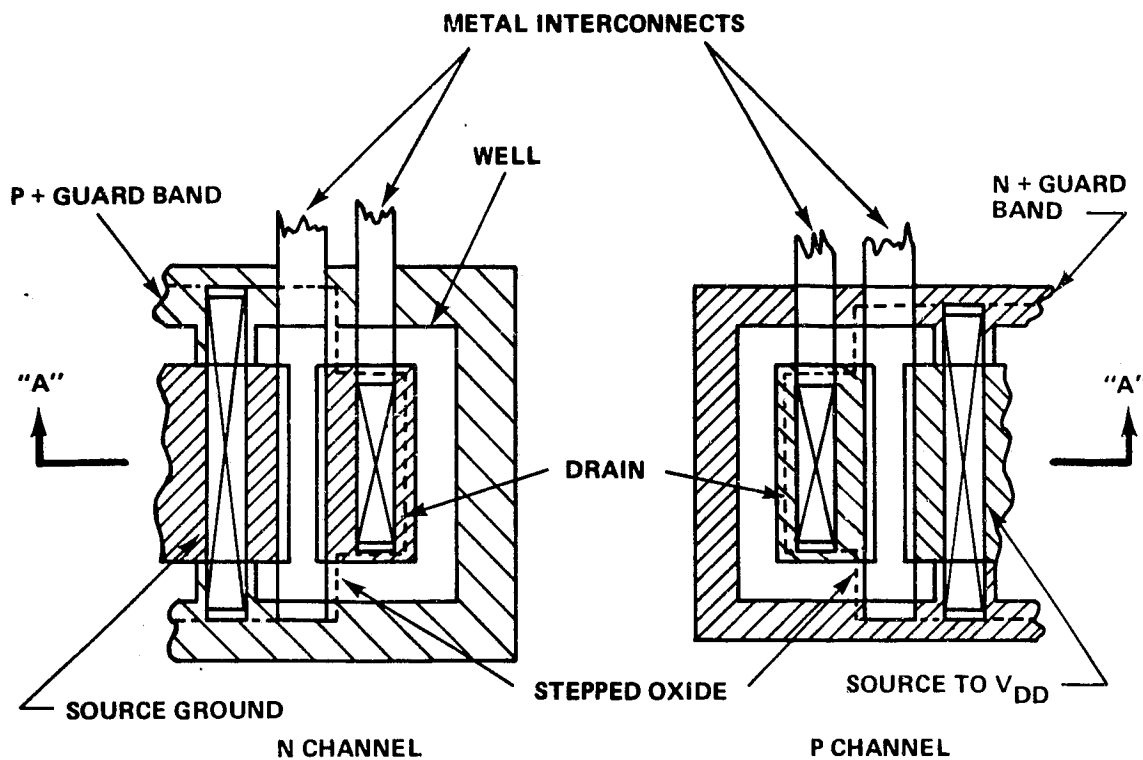
Specific design minimums for line widths and separations are shown in Figure 19(a). Since this drawing required dimensions for clarity, the scale has been increased to 1000X. Specific layout design rules are tabulated in the following. The letter pertaining to a particular rule is also shown on Figure 19(a) where applicable.

Device Source-Drain

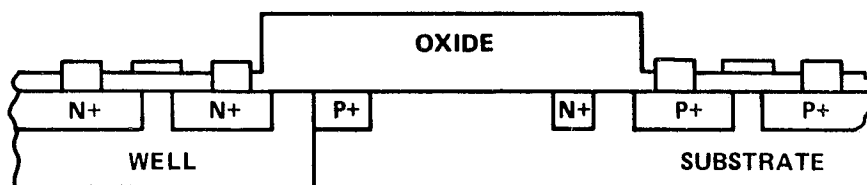
- A (1) Standard minimum device channel width — 0.7 mil.
- (2) Special minimum channel width — 0.4 mil [Fig. 19(b)].
- B Minimum source or drain diffusion width — 1.0 mil.
- C Minimum device channel length — 0.3 mil.

Contact Opening

- D Minimum contact width — 0.4 mil.
- E Minimum contact length — 0.3 mil. To minimize potential drops and corresponding loss in transconductance, contact openings for metallization should be made along the full length of device source and drain limited by rule F.
- F Minimum separation, contact opening to periphery of source or drain diffusion — 0.2 mil.



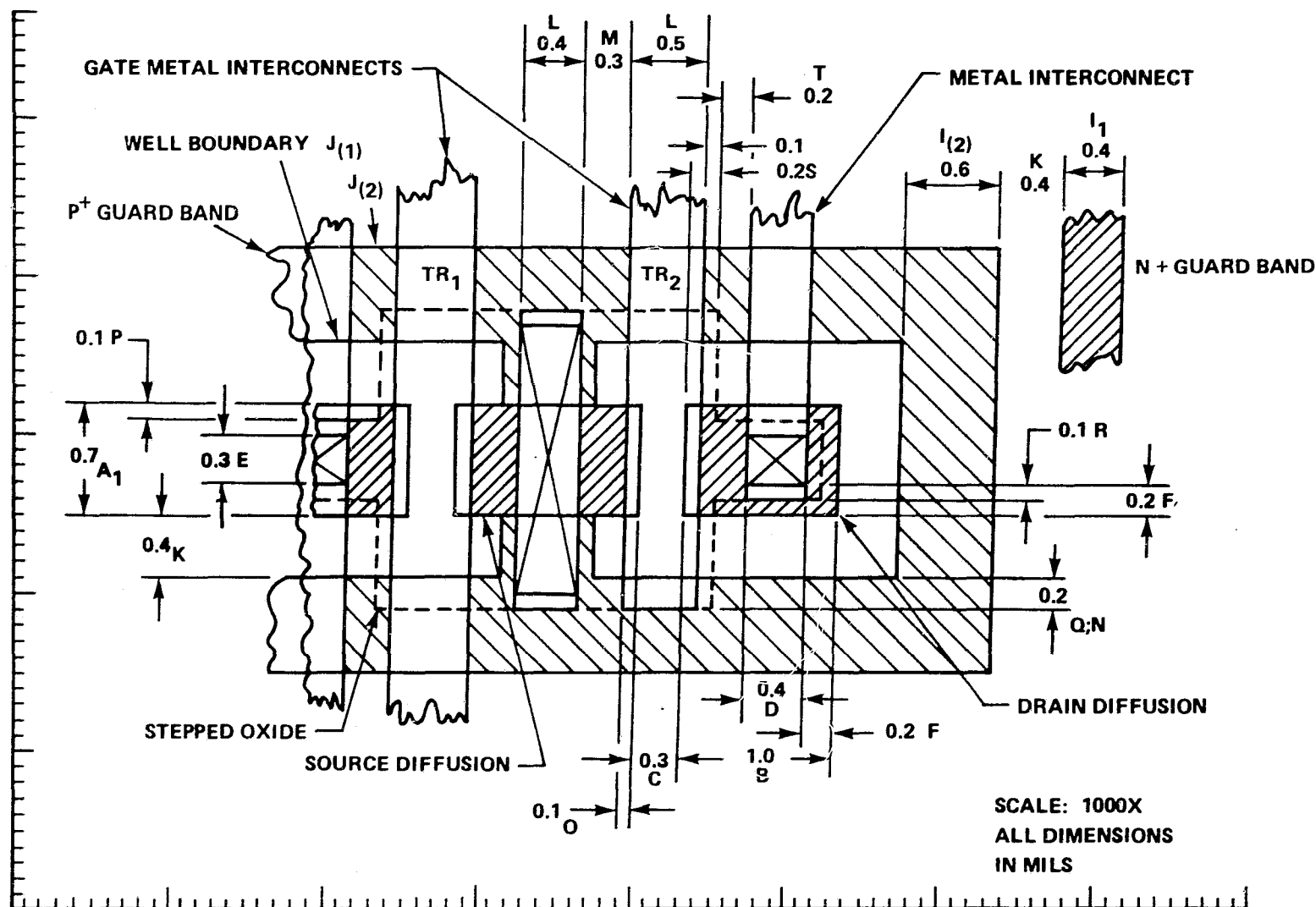
TOP VIEW SCALE - 500X



SECTION "A-A"

SECTION "A-A" NO SCALE

Figure 18. Typical N- and P-channel MOS complementary transistors.



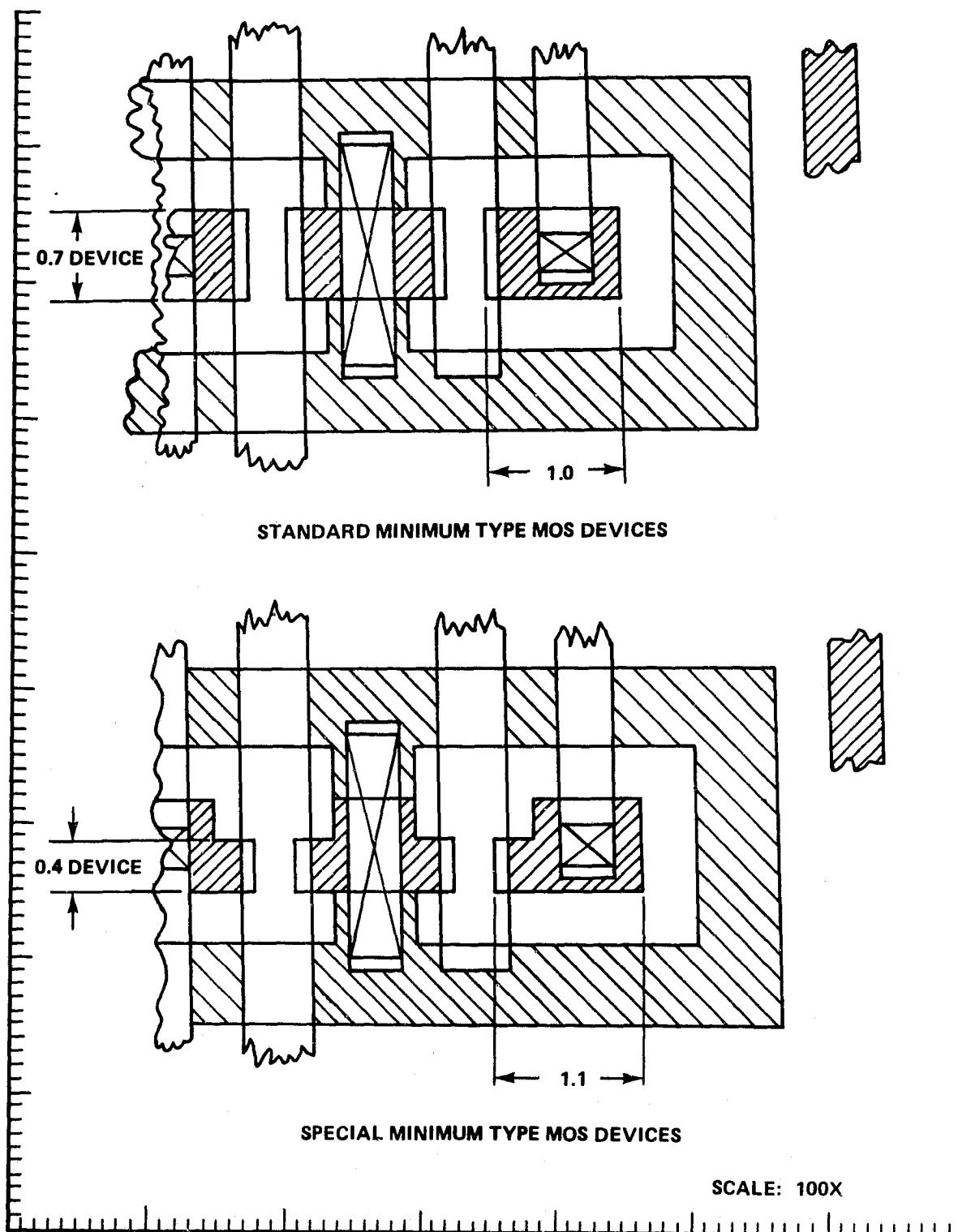


Figure 19(b). Minimum MOS transistors.

Metal-to-Contact Alignment

- G Alignment of metal width to contact opening of source or drain, line-to-line with both edges of contact.
- H Minimum overlap, metal over edge of contact opening to well, substrate, tunnels, diodes — 0.1 mil.

Guard Bands

- I Minimum guard band width:
- (1) Around N- and P-channel devices and P+ or N+ diodes — 0.4 mil.
 - (2) Around well — 0.6 mil.

Where space permits, it is preferred that guard bands be large diffused areas rather than narrow bands to minimize potential drops along the V_{DD} and ground supply lines when the guard bands are used as tunnels.

- J P+ guard band design for well:
- (1) Inside edge of P+ guard band must be at least line-to-line with well boundary or extend inside well for the additional purpose of service as a guard band for the N-channel and N+ diode devices, and as a tunnel for the ground supply.
 - (2) Outside edge of P+ guard band must extend at least 0.6 mil outside well boundary.
- K Minimum P+ to N+ separation — 0.4 mil. This rule primarily governs the clearance between guard bands and diffused areas.

Metal Interconnect

- L Minimum metal line width — 0.4 mil (except 0.5 mil for gates).
- M Minimum metal interconnect separation — 0.3 mil (except 0.4 mil for long, >10 mil, parallel metal lines).
- N Minimum metal gate, guard band overlap — 0.2 mil.

- O Minimum overlap, gate metal over source-drain channel — 0.1 mil.

Stepped Oxide

The stepped oxide is used to raise metal to a high level above the substrate in comparison to channel oxide levels, to reduce capacitance and inversion layer formation, and to minimize potential pinhole shorts or leakage. Openings in the stepped oxide are required at the device regions and where contact is to be made to a diode, tunnel, or guard band. Bond pads should be at the top level of the stepped oxide; however, it should be opened at the street area. Openings for the device area should be held to a minimum. The stepped oxide opening should be inside the outer edge of the source-drain diffusion, with the exception of a "notch" to permit the gate to cross a guard band at the channel oxide level. Refer to Figure 18 for typical stepped oxide placement.

- P Minimum separation of stepped oxide opening inside outer edge of source-drain diffusions — 0.1 mil.
- Q Minimum penetration of stepped oxide within guard band for metal gate crossover — 0.2 mil.
- R Minimum separation of stepped oxide around any contact opening — 0.1 mil.
- S Minimum separation of stepped oxide opening and any source-drain channel running parallel with it — 0.2 mil.
- T Minimum separation of stepped oxide opening and any metal interconnect outside of it — 0.2 mil.

General

- U It is preferable not to have superimposed lines between levels; therefore, the minimum line separation should be 0.1 mil, with the exceptions noted in rules G and J.

2. BONDING PAD DESIGN

Two types of bond pads are required: large pads to which wires are actually bonded, and smaller pads which are used for test probes. The following rules apply to bond pad design:

a. The minimum bond pad size is 4.0 by 4.0 mils; however, where space permits, pads should be 4 by 5 mils.

b. The minimum bond pad-to-pad clearance is 4.0 mils (5.0 mils is preferred).

c. The minimum clearance of the bond pad to the P+ diffused area is 2.0 mils; the minimum clearance of the bond pad to the N+ diffused area is 0.5 mil.

d. The minimum separation of the bond pad to the street area is 1.8 mils. The minimum clearance of the bond pad to the other metal interconnect on the whisker wire "tail" end is 2.0 mils.

e. The bond pads should be spaced uniformly around the periphery of the unit. Avoid concentrations of bond pads on only two or three sides of the unit.

f. The minimum test pad size is 1.5 by 1.5 mils.

3. STREET AREA DESIGN

The street area should be 4.0 mils wide. The overall chip size and reference X-Y axis should be computed from the centerline of the street area.

4. ALIGNMENT KEY DESIGN

A main alignment key should be located in each pattern, usually near the periphery of the pattern. The alignment is made by fitting a small sized opaque pattern within a larger size light pattern. Figure 20 provides dimensions for the main alignment key. Two additional alignment keys should be provided in each of the P+, N+, and metal patterns to facilitate the critical alignments of N+ to P+ and metal to both N+ and P+ individually. These keys are also shown in Figure 20. Alignment keys should be separated from the diffused active circuit area by a minimum of 0.5 mil.

5. TEST DEVICE DESIGN

Space allotment should be made in the layout of each pattern for separate N- and P-channel test transistors. The design of these test devices should follow standard layout design rules. Figure 17 is a design drawing for the standard test transistors which use a channel width of 2.0 mils. The location of these test

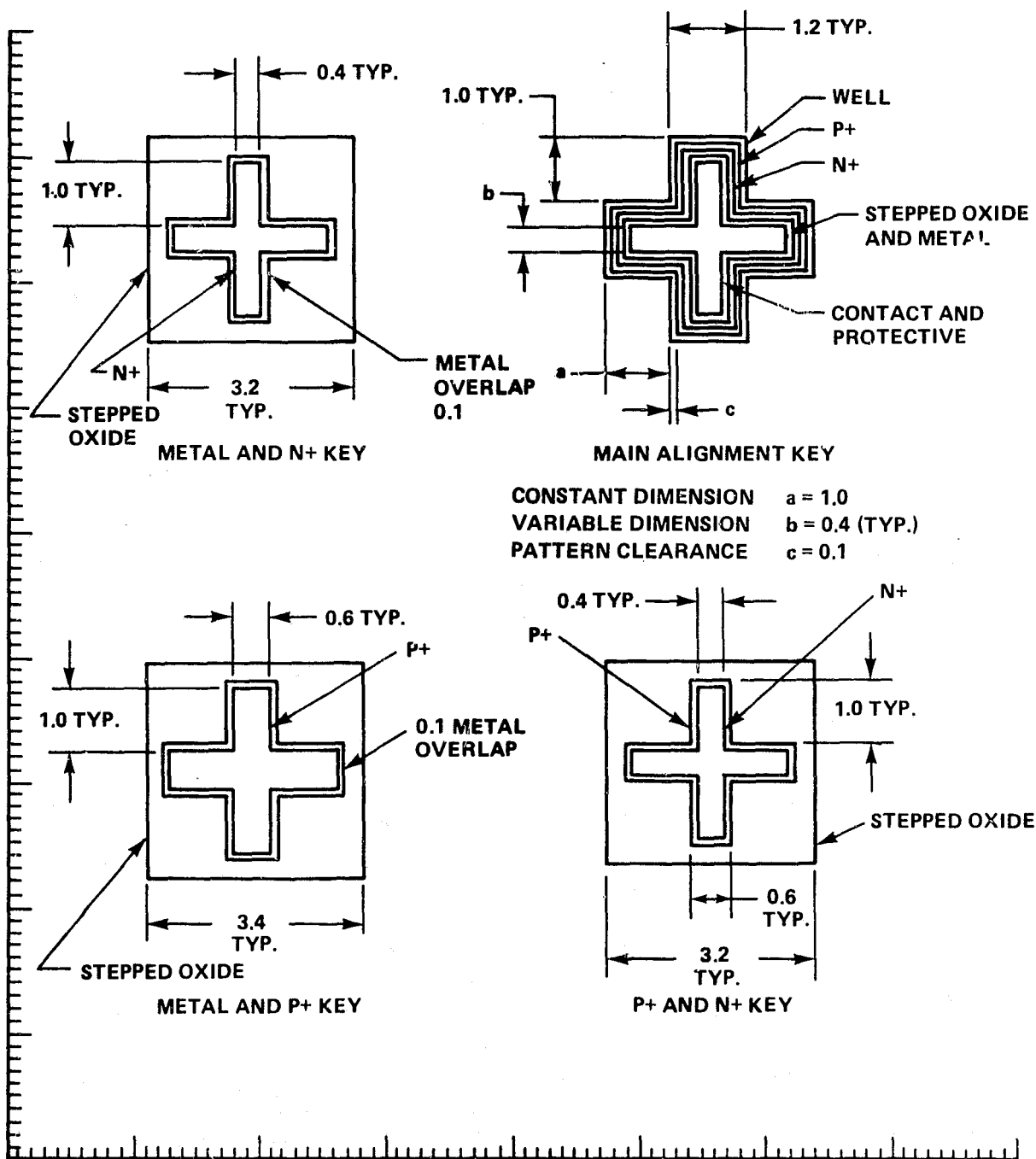


Figure 20. Alignment keys.

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OF POOR QUALITY

devices on the pattern layout is optional; however, the orientation of the test pads should be similar to facilitate probing the N- and P-channel transistors without interchanging probe wires and with a minimum of probe displacement.

6. PROTECTIVE BOND PAD MASK

A passivation layer is used to protect the overall circuit. This layer requires a mask to provide openings inside the bond pads. The openings should be 0.1 mil inside the bond pad boundary.

7. P-WELL SHEET RESISTANCE

A resistor with dimensions as indicated in Figure 16 should be incorporated on the Y-axis of the dice area on both sides of the P-well layout. This resistor permits direct measurement of the P-well sheet resistance at any point on any wafer by using the four-point probe technique. The area taken by this resistor should be protected against subsequent P+ and N+ diffusions and opened during the stepped oxide, contact, metal, and bond pad steps.

8. CIRCUIT IDENTIFICATION NUMBER

The prefix letter and three digits of the circuit identification number will normally be placed in the bottom X-axis street area of the P-well pattern and in the N-substrate area of the metal pattern between bond pads. The digits should be approximately 2 to 3 mils high and the width of the lettering should be approximately 0.3 mil.

IV. C-MOS STANDARD CELL LIBRARY

This section contains data sheets that describe the function, artwork, and performance of each of the standard cells in the MSFC complementary MOS bulk metal standard cell library, revision C. The data sheets and the supplemental information in this section will provide the system designer with sufficient information to optimize selection of the available standard circuits. On the reverse side of each cell data sheet is a pictorial representation of that cell. Each major grid line represents 1 mil on the chip; minor grid lines represent 0.5, 0.2, or 0.1 mil. One major grid line pair extends beyond the frame, thus pinpointing the location of the cell reference point. Each cell is identified by the technology code "C" and its cell number. The level is indicated below each frame. If no geometry is required on a particular level, the level

picture is not shown (dummy levels). Some cells require identical geometries on two or more levels. In this case the geometry is shown only once. The cell listing denotes such duplicate levels. The present C-MOS standard cells are listed in Table 1.

A. Cell Descriptions

1. TWO-, THREE-, AND FOUR-INPUT NOR's (1120, 1130, and 1140)

Two-, three-, and four-input NOR's (1120, 1130, and 1140) are group II functional circuits that provide the logical NOR operation. The four-input NOR cell has the largest device delay in this group. It may therefore be advisable to buffer the output of this cell before the total output node capacitance reaches 8 pF. Cells 1120 and 1130 are topologically interchangeable with cells 1720 and 1730, respectively.

2. TWO-, THREE-, AND FOUR-INPUT NAND's (1220, 1230, and 1240)

Two-, three-, and four-input NAND's (1220, 1230, and 1240) are group II functional circuits that provide the logical NAND operation. The four-input NAND cell has the largest device delay in this group. It may be advisable to buffer the output of the cell before the total output node capacitance reaches 8 pF. Cells 1220, 1230, and 1240 are topologically interchangeable with cells 1620, 1630, and 1640, respectively.

3. NONINVERTING BUFFER (1300)

Noninverting buffer (1300) is a group III cell that accomplishes its non-inverting function with two levels of inverting circuits. It is the recommended buffering circuit for those cells in group II that have heavy capacitive loads. The load at which it becomes advantageous to use cell 1300 varies for each cell in group II. However, an 8 pF load is suggested as a transition value.

4. BUFFER INVERTER (1310)

Buffer inverter (1310) is a group III functional circuit that provides the logical signal inversion and should be used where buffering is required (for loads greater than 8 pF). Cells 1310 and 1520 are interchangeable and logically identical.

TABLE 1. C-MOS STANDARD CELL LIBRARY LISTING

Cell No.	Function	Implementation	Drive Capability Group ^c	Cell Description, Section Paragraph	Dummy Level(s)	Duplicate Level(s)	Source
1120	2-Input NOR Gate	FL ^a	II	1	7	—	RCA
1130	3-Input NOR Gate	FL	II	1	7	—	RCA
1140	4-Input NOR Gate	FL	II	1	7	—	RCA
1220	2-Input NAND Gate	FL	II	2	7	—	RCA
1230	3-Input NAND Gate	FL	II	2	7	—	RCA
1240	4-Input NAND Gate	FL	II	2	7	—	RCA
1300	Noninverting Buffer	FL	III	3	7	—	RCA
1310	Buffer Inverter	FL	III	4	7	—	RCA
1320	Transmission Gate	TG ^b	I	5	7	—	RCA
1330	2-Input Transmission Gate	TG	I	6	7	—	RCA
1350	3-Input Transmission Gate	TG	I	7	7	—	RCA
1520	Double Buffer Inverter	FL	IV	8	7	—	RCA
1530	Double Buffer + Buffer Inverter	FL	IV/III	9	7	—	RCA
1620	2-Input AND Gate	FL	III	10	7	—	RCA
1630	3-Input AND Gate	FL	III	10	7	—	RCA
1640	4-Input AND Gate	FL	III	10	7	—	RCA
1720	2-Input OR Gate	FL	III	11	7	—	RCA
1730	3-Input OR Gate	FL	III	11	7	—	RCA
1800	4 × 2 Input AND + 4 × NOR Gate	FL	II	12	7	—	RCA
1820	D-Type Master/Slave Flip-Flop	FL	II	13	7	—	RCA
1830	D-Type Flip-Flop	FL	III	14	7	—	RCA
1840	3 × 3 Input AND + 3 × NOR Gate	FL	II	15	7	—	RCA
1860	2 × 2 Input AND + 4 × NOR Gate	FL	II	16	7	—	RCA
1870	2 × 2 Input AND + 2 × NOR Gate	FL	II	17	7	—	RCA
1880	2-Bit Carry Anticipate	FL	II	18	7	—	RCA
1890	3 × 2 Input AND + 3 × NOR Gate	FL	II	19	7	—	RCA
2310	2-Input Exclusive OR Gate	FL	III	20	7	—	RCA
9000	Top/Bottom Dummy Pad	N/A	N/A	21	1,2,4,5	—	MSFC
9010	Side Input Pad	N/A	N/A	21	—	—	MSFC

a. FL — Functional Logic

b. TG — Transmission Gate Logic

c. Groups are defined in Section II.

TABLE 1. (Concluded)

Cell No.	Function	Implementation	Drive Capability Group ^c	Cell Description, Section Paragraph	Dummy Level(s)	Duplicate Level(s)	Source
9020	Top/Bottom Output Pad	N/A	N/A	21	1	—	RCA
9030	Top/Bottom Input Pad	N/A	N/A	21	—	7=level 7 of Cell 9020	RCA
9040	Top/Bottom Pad With Pull-Up Resistor	N/A	N/A	21	—	—	MSFC
9050	Side Pad with Driver Inverter	N/A	N/A	21	—	—	MSFC
9070	Side Output Pad	N/A	N/A	21	1	—	MSFC
9080	Side Dummy Pad	N/A	N/A	21	1,2,4,5	—	MSFC
9100	Ground Pad	N/A	N/A	21	1,2,4,5	—	RCA
9110	V _{DD} Pad	N/A	N/A	21	1,2	—	RCA
9120	Long Ground Pad	N/A	N/A	21	1,2,4,5	—	MSFC
9210	On-Chip Alignment Mark	N/A	N/A	21	—	—	MSFC
9220	On-Chip Alignment Mark	N/A	N/A	21	1,2,5,7	—	MSFC
9230	On-Chip Alignment Mark	N/A	N/A	21	1,5,7	—	MSFC
9240	On-Chip Alignment Mark	N/A	N/A	21	1,6,7	—	MSFC
9250	Off-Chip Alignment Mark	N/A	N/A	21	—	2=4=5=7=lev. 1;6=lev. 3	RCA
9260	Off-Chip Alignment Mark	N/A	N/A	21	—	2=4=5=7=lev. 1;6=lev. 3	MSFC
9300	P- and N-Test Transistor	N/A	N/A	21	—	—	RCA
9310	P-Test Transistor	N/A	N/A	21	1	—	RCA
9320	N-Test Transistor	N/A	N/A	21	—	—	RCA
9400	Level Identification	N/A	N/A	21	—	—	MSFC
9410	Identification "NASA"	N/A	N/A	21	—	2=3=4=5=6=7=lev. 1	MSFC
9420	Identification "MSFC C" (All Levels)	N/A	N/A	21	—	2=3=4=5=6=7=lev. 1	MSFC
9430	Identification "MSFC C" (Level 6 Only)	N/A	N/A	21	1,2,3,4,5,7	6=level 1 of Cell 9420	MSFC
9440	Identification "C" (Level 6 Only)	N/A	N/A	21	1,2,3,4,5,7	—	MSFC
9450	Identification "MSFC" (Level 6 Only)	N/A	N/A	21	1,2,3,4,5,7	—	MSFC
9500	Feed-Through to P+ Diffusion	N/A	N/A	21	1,7	—	RCA
9510	Feed-Through to N+ Diffusion	N/A	N/A	21	1,2,3,7	—	MSFC
9600	End Cap	N/A	N/A	21	1,4,5,6,7	—	RCA
9700	Numeric Characters 0 to 9 (All Levels)	N/A	N/A	21	—	2=3=4=5=6=7=lev. 1	RCA
To 9790							
9800	Numeric Characters 0 to 9 (Level 6 Only)	N/A	N/A	21	1,2,3,4,5,7	6=level 1 of Cell group 9700/9790	MSFC
To 9890							

5. TRANSMISSION GATE (1320)

Transmission gate (1320) is a group I cell that has been implemented with transmission devices. The output of these gates may be tied together to provide an extra logic level. When control signal C is low (or 0), the gate is in the conducting state. Although the cell functions as a nonlinear resistor, at this time the effective "on" resistance can be accurately represented by a fixed 3 to 4 k Ω resistor. The dynamic "on" resistance may be reduced by paralleling two or more such devices. When control signal C is high (or 1), the gate is in the nonconducting state. This places the output node in a floating or undefined state. Therefore, caution should be exercised when using this cell. Generally longer delay times result when the control line is used to clock a waiting input signal through the cell. The primary purpose of the circuit is to permit multiple access to system busses.

6. SINGLE CLOCK, DUAL TRANSMISSION GATE — MULTIPLEXER (1330)

This cell furnishes the designer with a 2 to 1 electronic relay switch. It is mechanized with transmission gate devices and therefore is a group I circuit. When the control signal C is low (or 0), the relay path B-X is conducting. When the control signal C is high (or 1), the relay path A-X is conducting. Hence, a high control signal connects the "dotted" input terminal to the output. Because the output node X is always connected to one and only one input node, the output is always defined. Therefore it is generally not possible to tie the output of this cell to the output of another cell. Although the cell functions as a nonlinear resistor, when conducting the effective "on" resistance may be accurately represented by a fixed 1 to 2 k Ω resistor.

7. TRIPLE CLOCK, TRIPLE TRANSMISSION GATE — MULTIPLEXER (1350)

This is a group I cell which provides a 3 to 1 electronic relay switch. When any one of the control signals (C_1 , C_2 , or C_3) is low, one of the relay paths (D1-X, D2-X, or D3-X) is conducting. For example when C_2 is low, the relay path D2-X is conducting. When all three control signals (C_1 , C_2 , and C_3) are high (or 1), the output is in a "floating" or undefined state. The ability to put all three data relays into the nonconducting state, and thereby permit the output node to float, provides the capability to wire-OR the output of this cell. Cell 1320 also provides this capability. Caution must be exercised to ensure that at no time are any two (or three) control signals simultaneously low. This condition can cause an indeterminate output state. When conducting, each relay functions as a nonlinear resistor; the effective "on" resistance may be approximated by a fixed 1 to 2 k Ω resistor.

8. DOUBLE BUFFER INVERTER (1520)

Double buffer inverter (1520) is a group IV cell that should be used in those cases where a large amount of buffering is required (for loads in excess of 25 pF). Cell 1520 is the largest buffering circuit presently in the library. When additional buffering is required, two or more 1520 cells may be connected in parallel. Inverter cells 1310 and 1520 are functionally identical, although they have different driving capabilities.

9. DOUBLE BUFFER/BUFFER INVERTER (1530)

This cell provides both an inverting and a noninverting operation. The inverting output is in drive capability group IV, while the noninverting output is in drive capability group III. From the data sheet, it is clear that the propagation delay A-Y depends upon the loads at node X and node Y. Using this cell in place of the individual logic gates (1310 and 1520) yields a 30 percent savings in area.

10. TWO-, THREE-, AND FOUR-INPUT AND's (1620, 1630, and 1640)

These provide, with two stages of functional circuitry, the logical AND operation. Each cell is a member of drive capability group III and should therefore be used for loads less than 25 pF. Cells 1620, 1630, and 1640 are topologically interchangeable with cells 1220, 1230, and 1240. This permits the interchange of NAND and AND functions at later stages in the array design.

11. TWO- AND THREE-INPUT OR's (1720 and 1730)

These provide, with two stages of functional circuitry, the logical OR operation. Each cell is a member of drive capability group III and should therefore be used for loads less than 25 pF. Cells 1720 and 1730 are topologically interchangeable with cells 1120 and 1130. This permits the interchange of NOR and OR functions at later stages in the array design.

12. 4×2 INPUT AND + $4 \times$ NOR GATE (1800)

This is a specialized cell that utilizes functional logic to implement a logical operation that would otherwise require at least five basic standard cells. Using this cell in place of the individual logic gates produces: (a) a considerable savings in chip area and (b) a slightly longer stage delay. The complexity of the topological construction of the cell has placed it among the slower members of drive capability group II.

13. D-TYPE MASTER/SLAVE FLIP-FLOP (1820)

This cell has been implemented with a configuration of functional and transmission gate logic. The transmission devices are used only to connect or disconnect each flip-flop from its preceding circuitry. As can be seen from the data sheet, each flip-flop is implemented with two inverters of unequal size. The feedback (or dashed) inverter has less than one-tenth the drive power of a standard group II circuit. It is therefore incapable of opposing any logical voltage level placed at the data input terminal D. When the input transmission device is conducting (control signal C is high), the logical level placed at the data input will automatically force the output of the dashed inverter into the same state. Once the effects of this forced state have propagated through the larger (solid lines) inverter, flip-flop latch-up will occur. At this time, the output (or slave) flip-flop is isolated from the input (or master) flip-flop by way of the nonconducting transmission gate. The feedback inverter serves two purposes: (a) it permits data to be stored indefinitely and independently of clock frequency, and (b) it improves the noise immunity at the input to each flip-flop.

When the control signal goes from high to low (1 to 0), the data stored in the master flip-flop will be transferred through the internal transmission gate to the slave flip-flop. In a manner similar to that just described, the feedback inverter of the slave flip-flop will be forced to the desired state. The slave flip-flop will then latch-up. During a portion of the transition time of the control signal, both transmission devices will be conducting. However, the circuits have been so designed that the inherent delays associated with the transmission devices and the flip-flop latch-up will guarantee proper operation over the entire voltage range.

In summary, the information on input line D may be loaded into the master flip-flop when the signal on control line C is held high. The information stored in the master may be transferred to the slave flip-flop, and hence to the output, by bringing the control line low.

The minimum recommended positive-going clock pulse width required to load the master flip-flop is 70 ns. The minimum negative clock width for several loading conditions is specified on the data sheet. It is recommended that the data line be held constant for at least 50 ns prior to and succeeding all clock transitions.

14. D-TYPE FLIP-FLOP (1830)

This cell has been implemented with functional and transmission gate logic. The transmission device is used only to connect or disconnect the flip-flop from its preceding circuitry. As shown in the data sheet, the flip-flop is implemented with two inverters of unequal size. The feedback (or dashed) inverter has less than one-tenth the drive power of a standard group II circuit. It is therefore incapable of opposing any logical voltage level placed at data input terminal D. When the input transmission device is conducting (control signal C is low), the logical level placed at the data input will automatically ripple through the inverter and set the flip-flop. The output of this flip-flop is buffered with an inverter in drive capability group III. The feedback inverter serves two purposes: (a) it permits data to be stored indefinitely and independently of clock frequency, and (b) it improves the noise immunity at the input to the flip-flop.

When the control signal goes from high to low (1 to 0), the data at the input is transferred through the transmission gate to the flip-flop. After a slight delay, it then appears at the output of the cell. When the control signal is high, the flip-flop is isolated from all preceding circuitry. When the control signal is low, the 1830 cell is essentially a combinatorial circuit. During a portion of the transition time of the control signal, the transmission device will be conducting. Therefore, it is mandatory that the input data line be held constant for at least 50 ns prior to and succeeding all clock transitions.

15. $1/2$, 2 AND -2NOR (1840)

This cell is a group II specialized cell that utilizes functional logic to implement the logical operation shown in the data sheet.

16. 2, 2 AND - 4 NOR (1860)

This cell is a group II specialized cell that utilizes functional logic to implement the logical operation shown in the data sheet.

17. 2×1 MULTIPLEXER (1870)

This cell is a group II specialized cell that utilizes functional logic to implement the logical operation shown in the data sheet.

18. TWO-BIT CARRY ANTICIPATE (1880)

This cell is a group II specialized cell that utilizes functional logic to implement a logical operation that would otherwise require at least three basic standard cells. Using this cell in place of the individual logic gates has two advantages: (a) less chip area is required, and (b) a faster stage delay is obtained. The circuit's primary application is in arithmetic units where it is used to reduce the carry ripple time of a parallel adder.

19. 3×1 MULTIPLEXER (1890)

This cell is a group II specialized cell that utilizes functional logic to implement the logical operation shown in the data sheet.

20. EXCLUSIVE-OR (2310)

This cell generates the required logical operation by utilizing a unique interconnection of four transistors. Although the cell is essentially a transmission gate arrangement, it is a group III cell because of its buffered output. It is recommended however that cell 2310 be further buffered, with a cell from group IV, when the output load exceeds 15 pF. Analysis has revealed an unequal propagation delay for the two inputs of the cell with input B providing the smaller propagation delay.

21. 9000 SERIES CELLS

The remaining standard cells are referred to as 9000 series cells and are miscellaneous in their application.

a. For Inputting and Outputting Electrical Signals and Power

9000 — Top or bottom dummy pad

9010 — Input pad with a 1.1 k Ω series resistor and input diode protection

9020 — Top or bottom output pad

9030 — Shorter version of cell 9010

9040 — Top or bottom input pad with a 3 k Ω pull-up resistor to V_{DD} and input diode protection

9050 — Side output pad with a driver inverter for driving large off-chip loads

9070 — Side output pad

9080 — Side dummy pad

9100 — Ground pad

9110 — V_{DD} pad

9120 — Long ground pad.

b. Alignment Mark Cells

9210 — On-chip alignment mark

9220 — On-chip alignment mark

9230 — On-chip alignment mark

9240 — On-chip alignment mark

9250 — Off-chip alignment mark

9260 — Off-chip alignment mark.

c. Test Transistors

9300 — P- and N-test transistor

9310 — P-test transistor

9320 — N-test transistor.

d. Identification Cells

9400 — Level identification

9410 — Identification "NASA"

9420 — Identification "MSFC C" (all levels)

- 9430 — Identification "MSFC C" (level 6 only)
- 9440 — Identification "C" (level 6 only)
- 9450 — Identification "MSFC" (level 6 only).
- e. Feed-Through Cells and Cell Row End Cap
 - 9500 — Feed-through to P+ diffusion
 - 9510 — Feed-through to N+ diffusion
 - 9600 — Cell row end cap.
- f. Numeric Characters
 - 9700 to 9790 — Numeric characters 0 to 9 (all levels)
 - 9800 to 9890 — Numeric characters 0 to 9 (level 6 only).

B. C-MOS Standard Cell Data Sheets and Pictorial Representations

Data sheets and pictorial representations for all cells in the C-MOS standard cell library are contained in the following pages. The complete library is listed in Table 1.

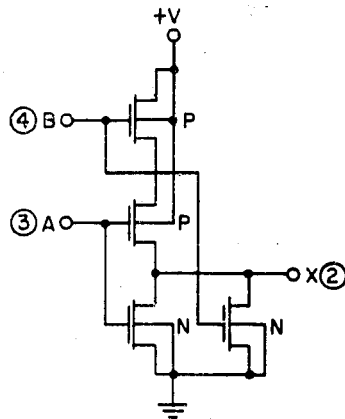
TWO-INPUT NOR

4 Devices
3 Pads

Cell Width = 5.8 mils

C-MOS STANDARD
CELL NO. 1120

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

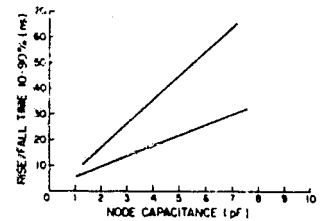
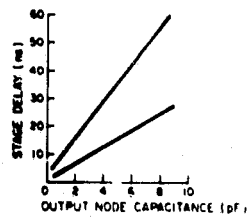
$$X = \overline{A + B}$$

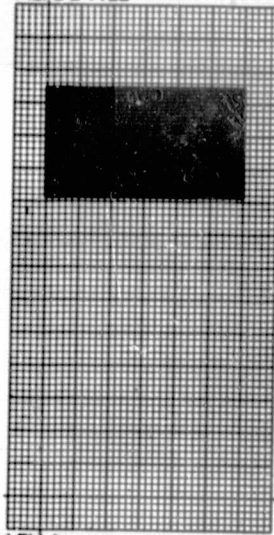
TRUTH TABLE

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

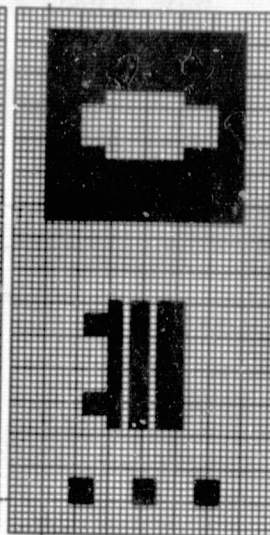
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.82
3	1.30
4	1.30

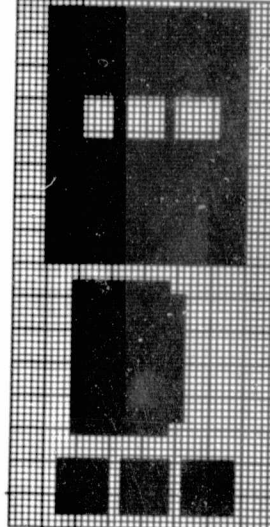




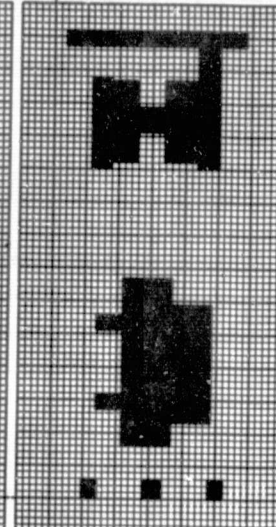
LEV 1



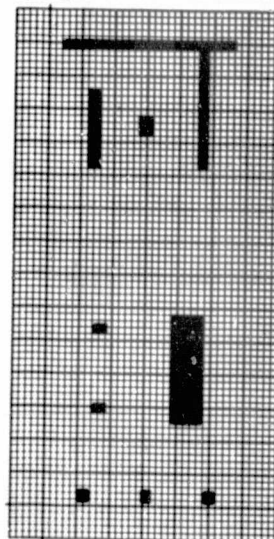
LEV 2



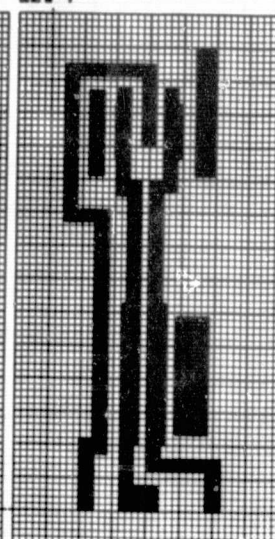
LEV 3



LEV 4



LEV 5



LEV 6

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THREE-INPUT NOR

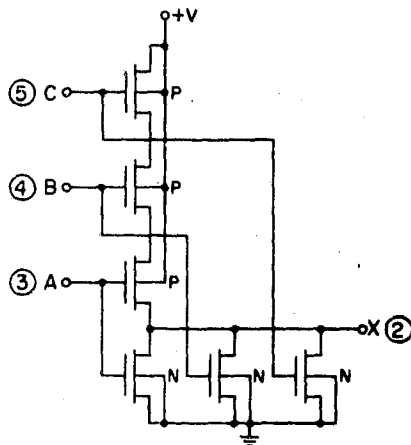
6 Devices

4 Pads

C-MOS STANDARD
CELL NO. 1130

Cell Width = 7.7 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

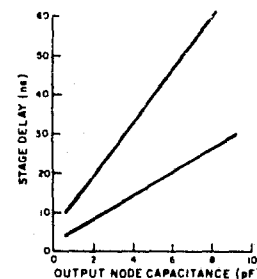
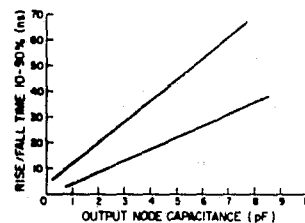
$$X = \overline{A \cdot B \cdot C}$$

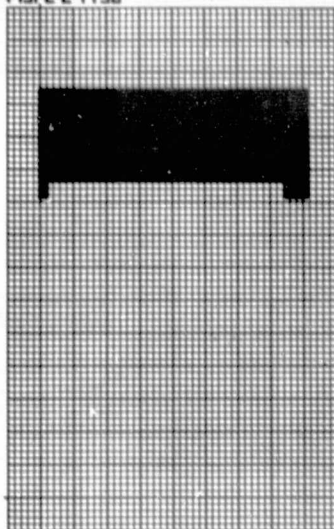
TRUTH TABLE

A	B	C	X
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

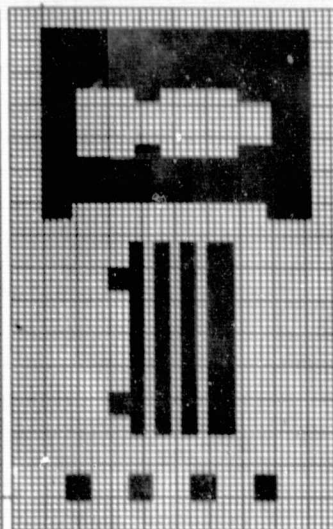
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.18
3	1.71
4	1.71
5	1.71

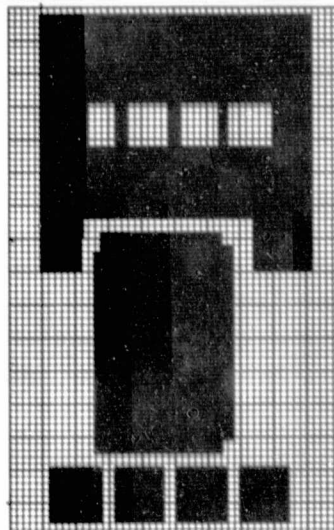




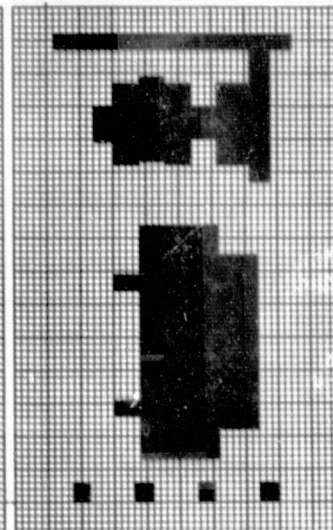
LEV 1



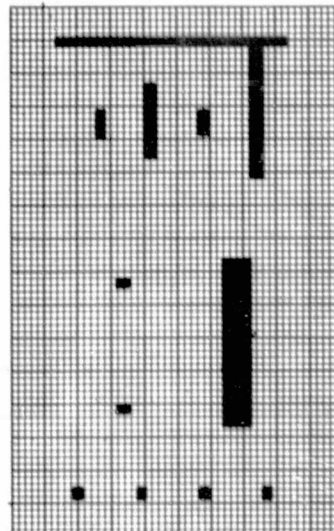
LEV 2



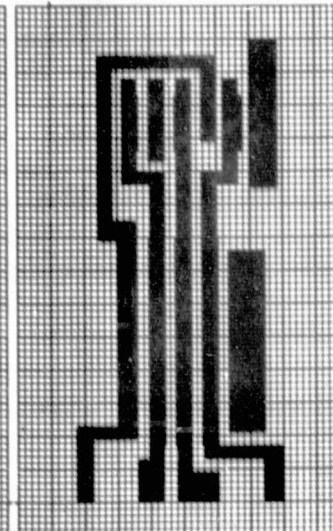
LEV 3



LEV 4



LEV 5



LEV 6

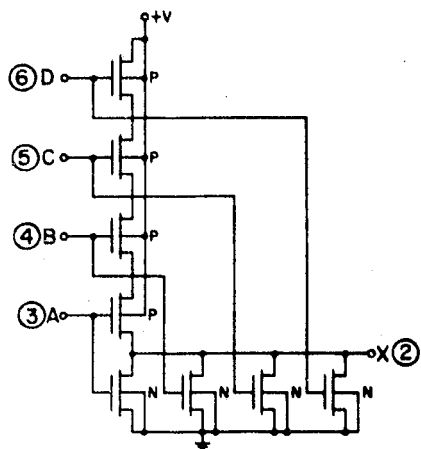
FOUR-INPUT NOR

8 Devices
5 Pads

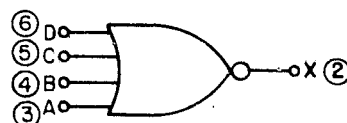
Cell Width = 9.6 mils

C-MOS STANDARD
CELL NO. 1140

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

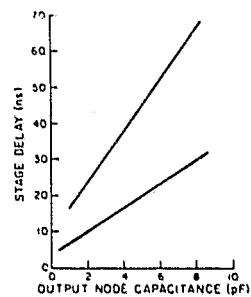
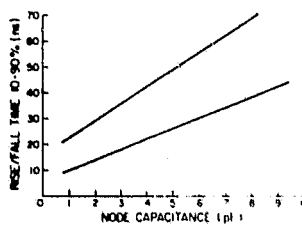
$$X = \overline{A + B + C + D}$$

TRUTH TABLE

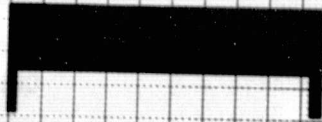
A	B	C	D	X
0	0	0	0	1
All other input combinations				0

CELL I/O CAPACITANCE VALUES

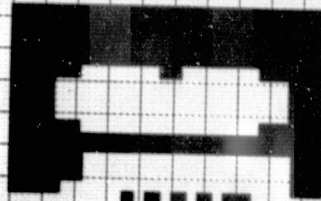
PIN	CAPACITANCE (pF)
2	1.39
3	1.82
4	1.82
5	1.82
6	1.82



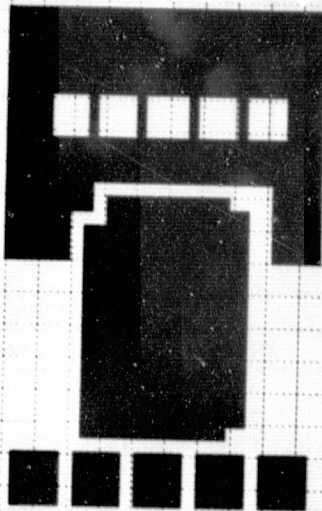
MSFC C 1140



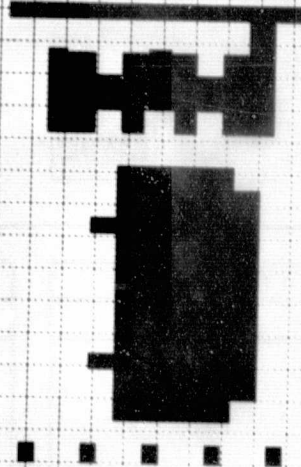
LEV 1



LEV 2



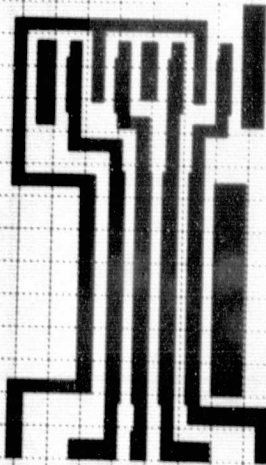
LEV 3



LEV 4



LEV 5



LEV 6

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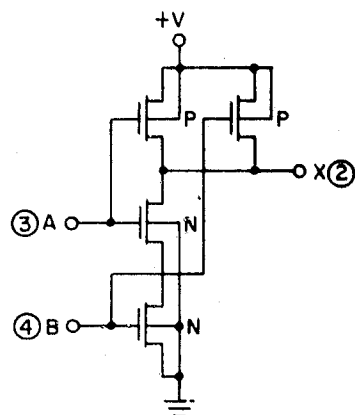
TWO-INPUT NAND

4 Devices
3 Pads

Cell Width = 5.8 mils

C-MOS STANDARD CELL
CELL NO. 1220

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

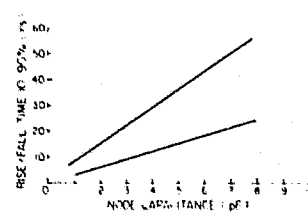
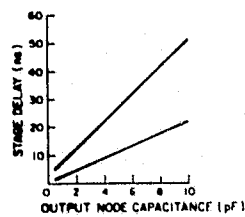
$$X = \overline{A \cdot B}$$

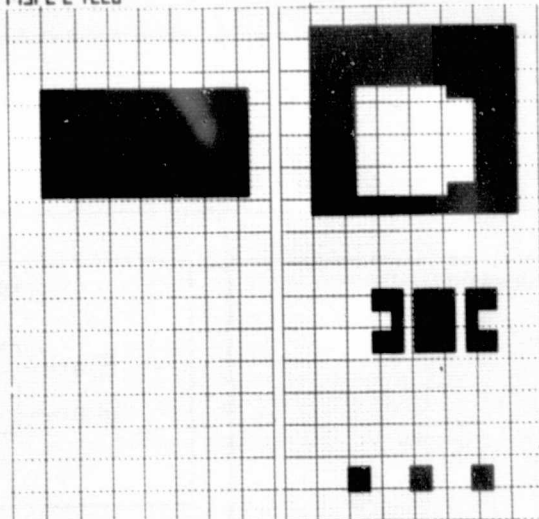
TRUTH TABLE

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

CELL I/O CAPACITANCE VALUES

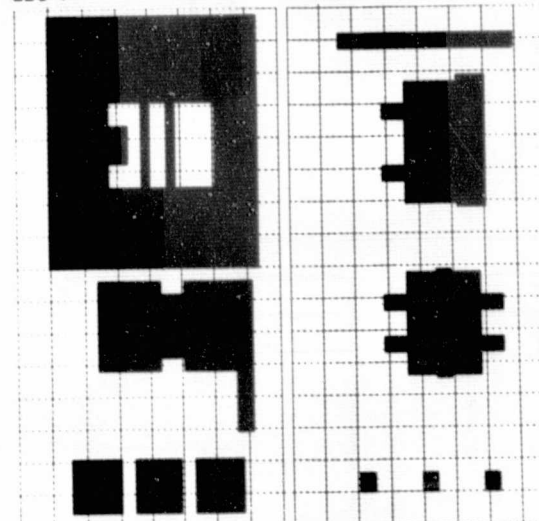
PIN	CAPACITANCE (pF)
2	1.04
3	1.17
4	1.17





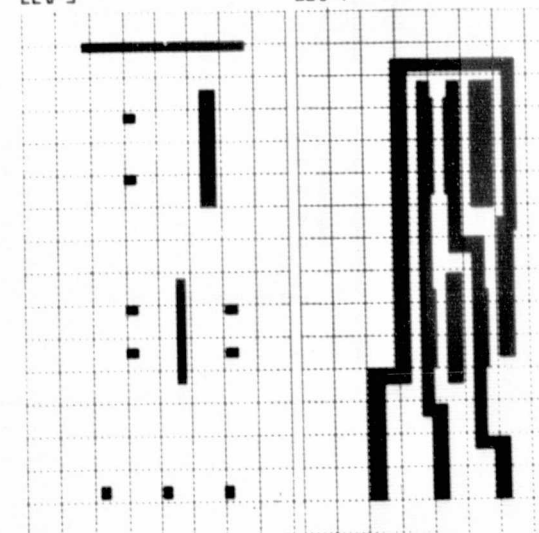
LEV 1

LEV 2



LEV 3

LEV 4



LEV 5

LEV 6

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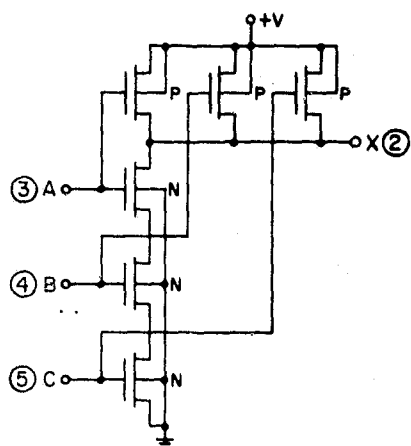
THREE-INPUT NAND

6 Devices
4 Pads

Cell Width = 7.7 mils

C-MOS STANDARD CELL
CELL NO. 1230

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

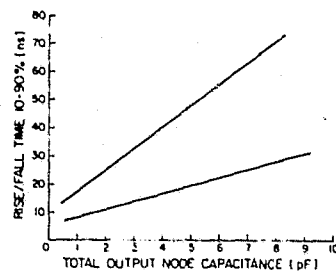
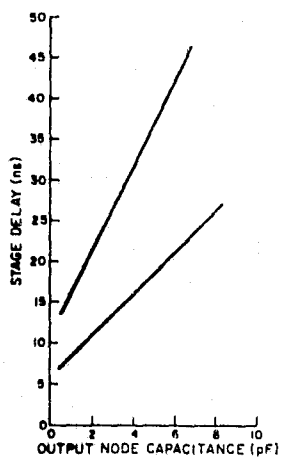
$$X = \overline{A \cdot B \cdot C}$$

TRUTH TABLE

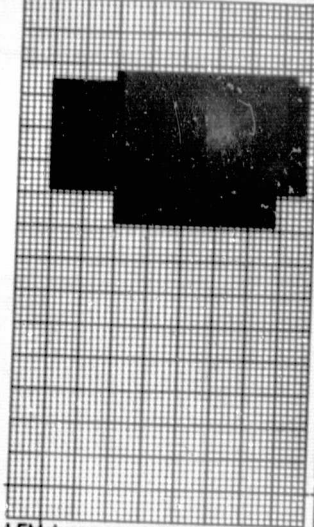
A	B	C	X
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

CELL I/O CAPACITANCE VALUES

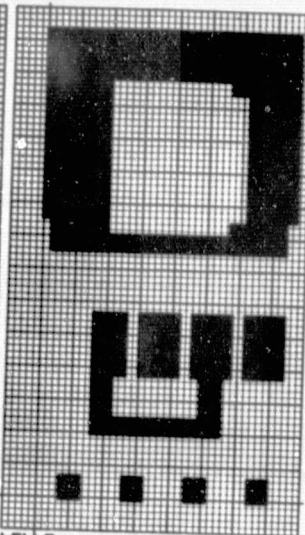
PIN	CAPACITANCE (pF)
2	0.76
3	1.40
4	1.40
5	1.40



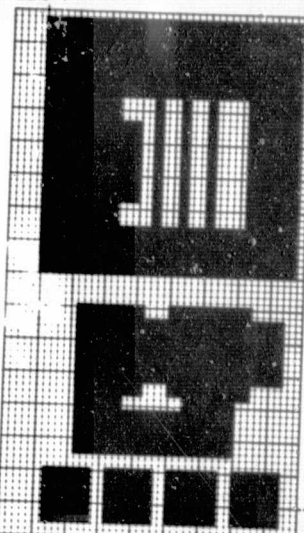
MSFC C 1230



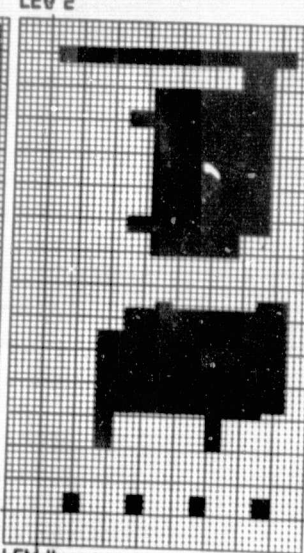
LEV 1



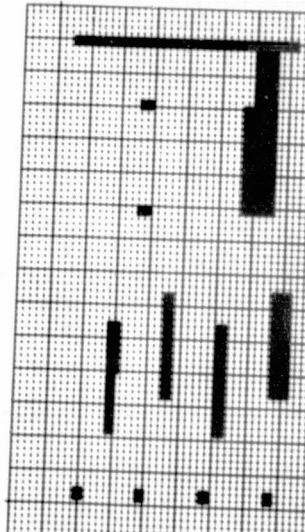
LEV 2



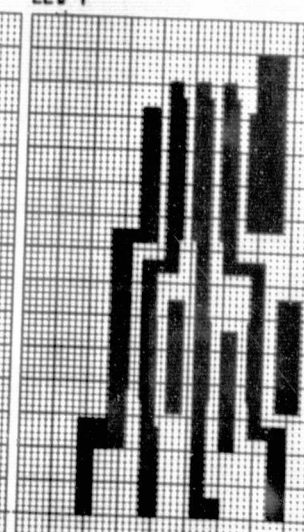
LEV 3



LEV 4



LEV 5



LEV 6

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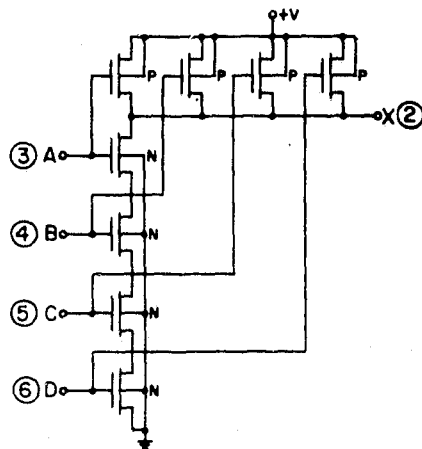
FOUR-INPUT NAND

8 Devices
5 Pads

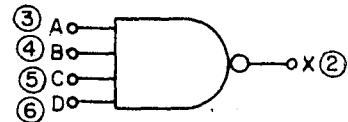
Cell Width = 9.6 mils

C-MOS STANDARD CELL
CELL NO. 1240

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

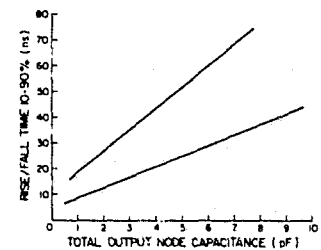
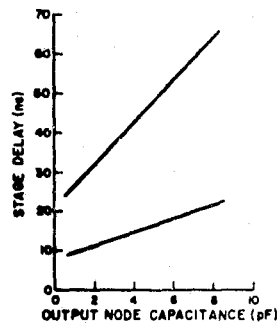
$$X = \overline{A \cdot B \cdot C \cdot D}$$

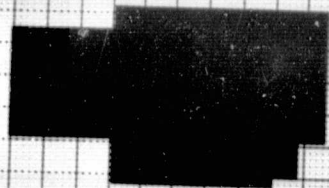
TRUTH TABLE

A	B	C	D	X
1	1	1	1	0
All other input combinations				1

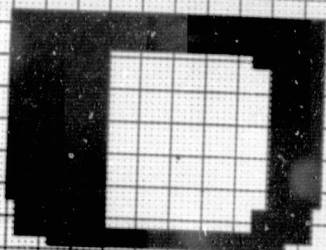
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.85
3	1.54
4	1.54
5	1.54
6	1.54

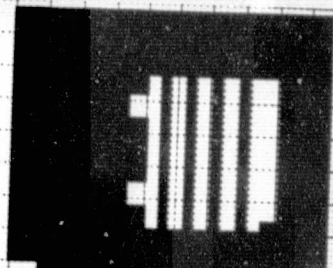
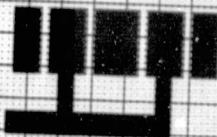




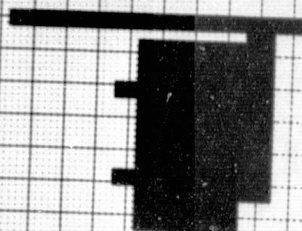
LEV 1



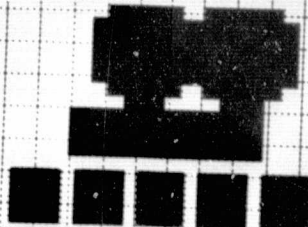
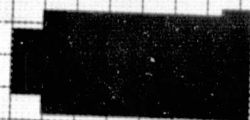
LEV 2



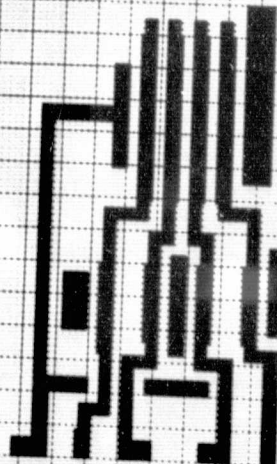
LEV 3



LEV 4



LEV 5



LEV 6

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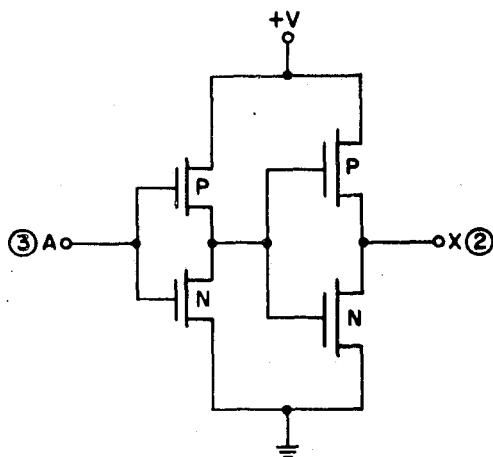
NON-INVERTING BUFFER

4 Devices
2 Pads

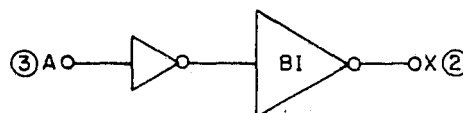
Cell Width = 4.5 mils

C-MOS STANDARD CELL
CELL NO. 1300

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

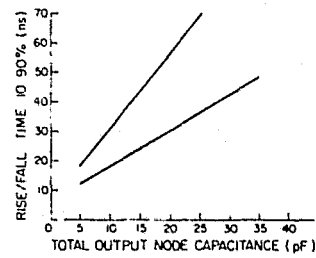
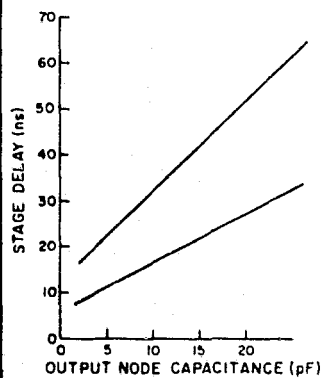
$$X = A$$

TRUTH TABLE

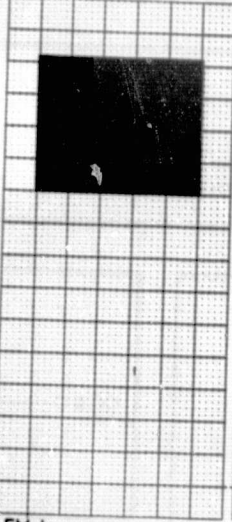
A	X
0	0
1	1

CELL I/O CAPACITANCE VALUES

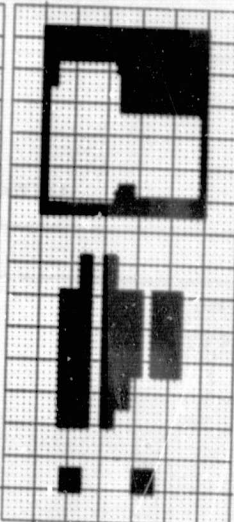
PIN	CAPACITANCE (pF)
2	1.36
3	1.17



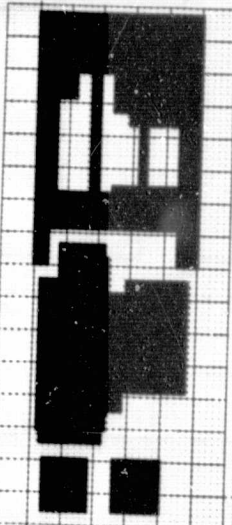
MSFC C 1300



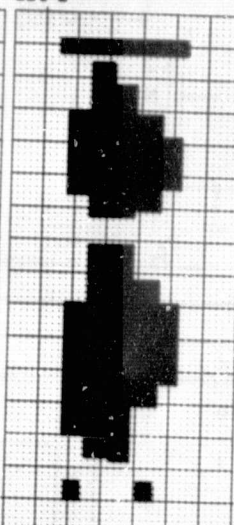
LEV 1



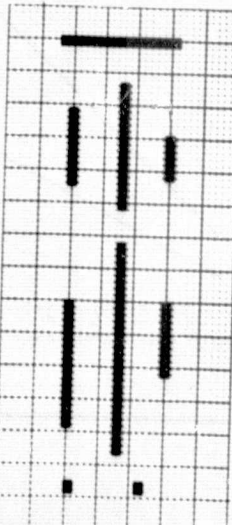
LEV 2



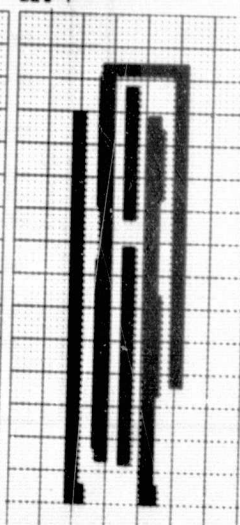
LEV 3



LEV 4



LEV 5



LEV 6

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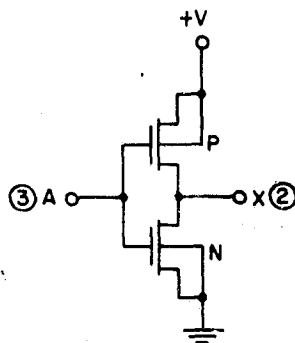
BUFFER INVERTER

2 Devices
2 Pads

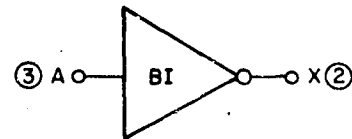
Cell Width = 3.9 mils

**C-MOS STANDARD
CELL NO. 1310**

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \overline{A}$$

TRUTH TABLE

A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.21
3	1.76

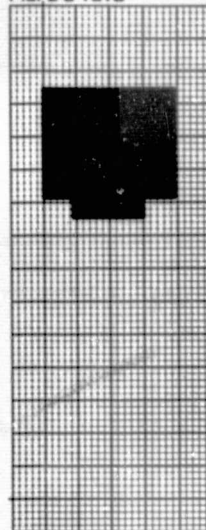
RISE/FALL TIME 10-90% (ns)

TOTAL OUTPUT NODE CAPACITANCE (pF)

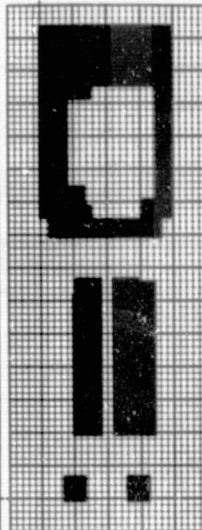
STAGE DELAY (ns)

OUTPUT NODE CAPACITANCE (pF)

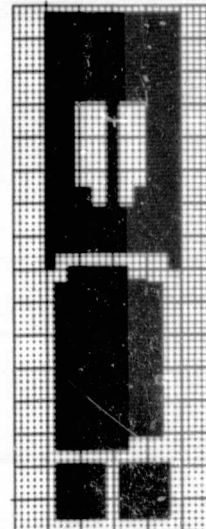
MSFC C 1310



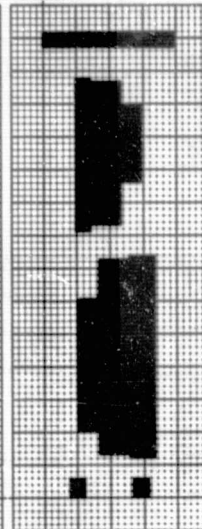
LEV 1



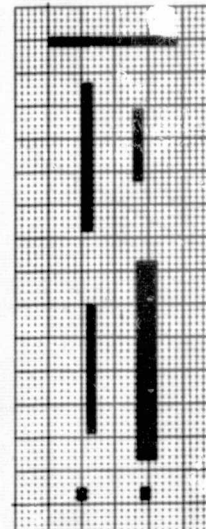
LEV 2



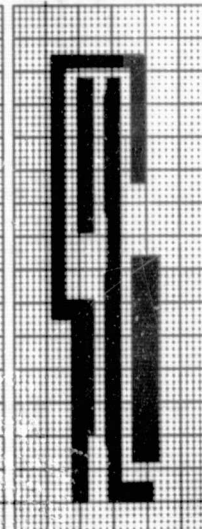
LEV 3



LEV 4



LEV 5



LEV 6

ORIGINAL PAGE IS
OF POOR QUALITY

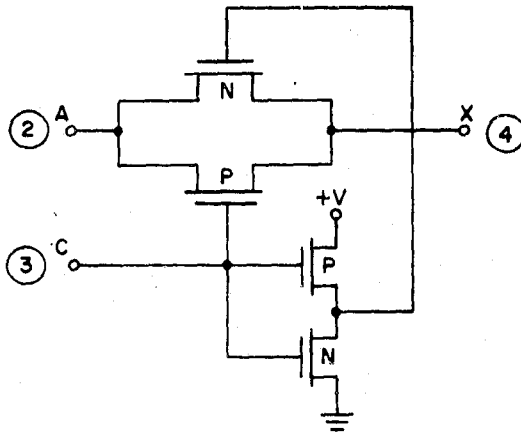
TRANSMISSION GATE

4 Devices
3 Pads

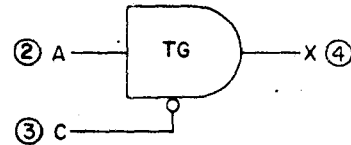
Cell Width = 5.7 mils

C-MOS STANDARD CELL
CELL NO. 1320

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = AC$$

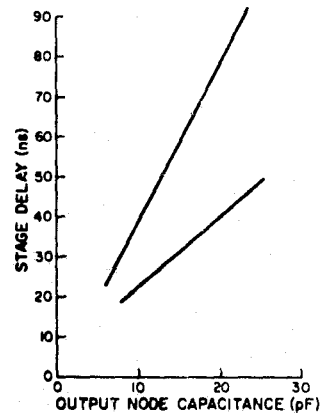
TRUTH TABLE

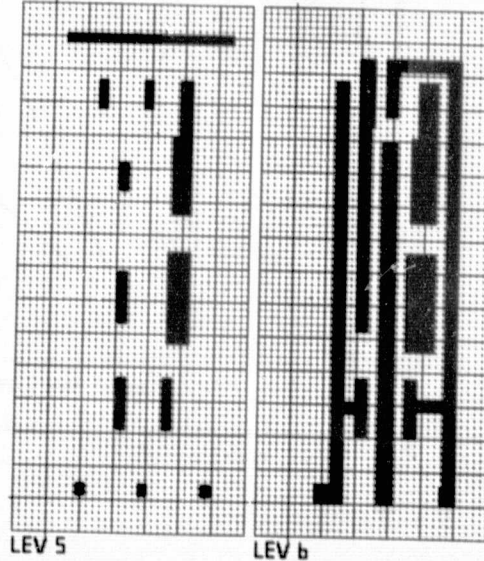
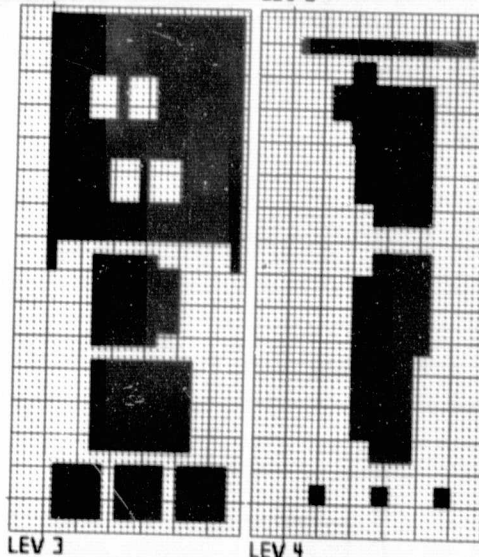
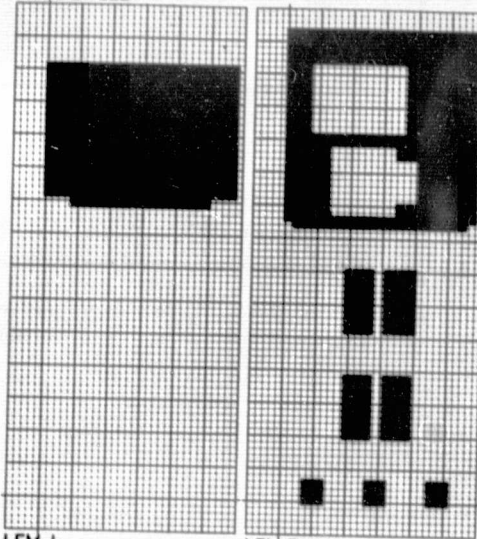
A	C	X
0	0	0
0	1	*
1	0	1
1	1	*

* Output is Undefined

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.62
3	1.15
4	0.62





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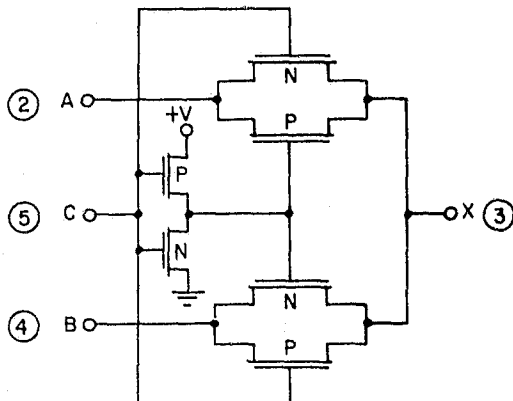
SINGLE CLOCK DUAL TRANSMISSION GATE (MULTIPLEXER)

C-MOS STANDARD
CELL NO. 1330

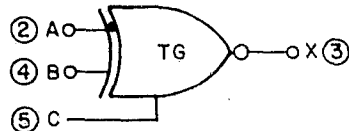
6 Devices
4 Pads

Cell Width = 7.7 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

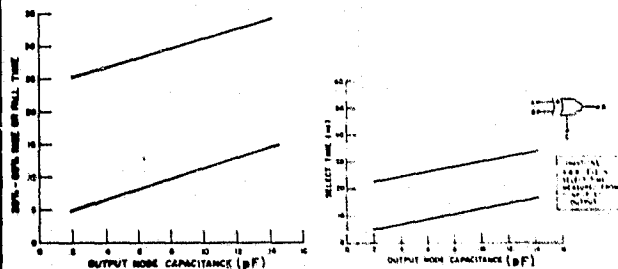
$$X = AC + \bar{C}B$$

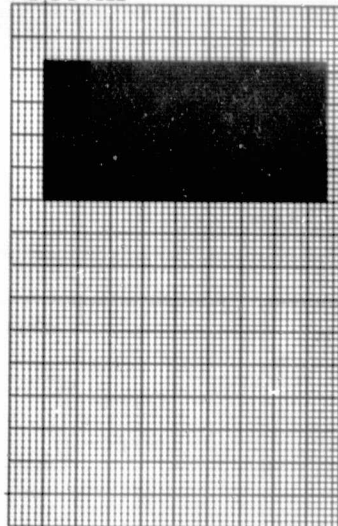
TRUTH TABLE

A	B	C	X
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	0
1	0	1	1
1	1	0	1
1	1	1	1

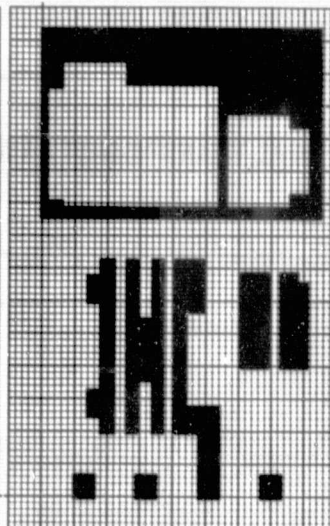
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.37
3	1.34
4	1.37
5	2.32

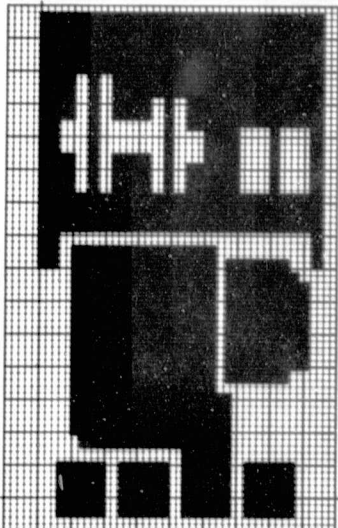




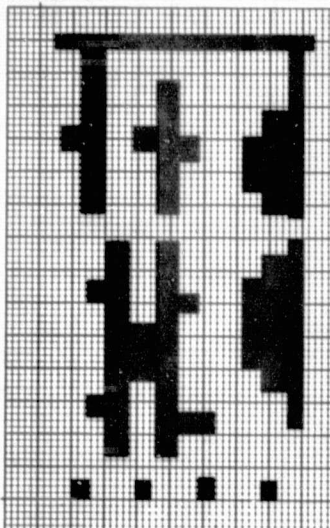
LEV 1



LEV 2



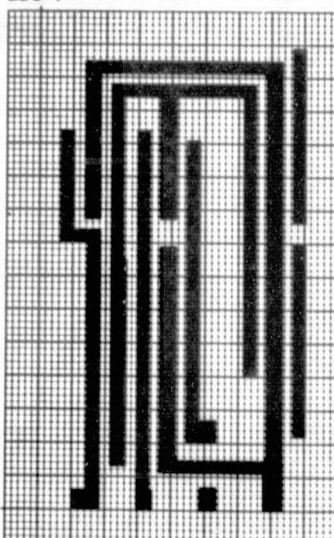
LEV 3



LEV 4



LEV 5



LEV 6

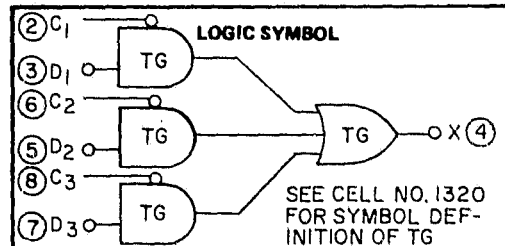
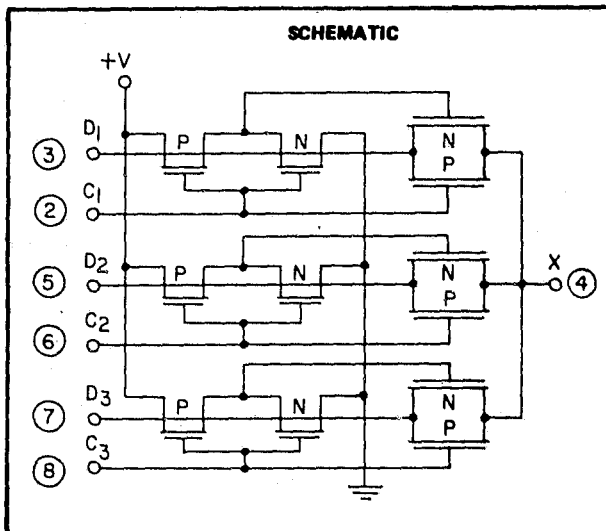
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TRIPLE CLOCK, TRIPLE TRANSMISSION GATE

C-MOS STANDARD
CELL NO. 1350

12 Devices
7 Pads

Cell Width = 15.4 mils



LOGIC EQUATION

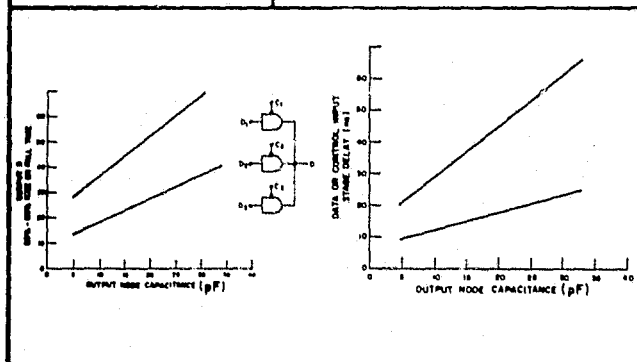
$$X = \overline{C_N} D_N$$

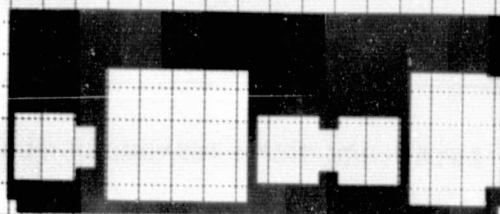
TRUTH TABLE

C ₁	C ₂	C ₃	X
0	0	0	Illegal and Undefined
0	0	1	"
0	1	0	"
1	0	0	"
1	1	0	D3
1	0	1	D2
0	1	1	D1
1	1	1	Undefined

CELL I/O CAPACITANCE VALUES

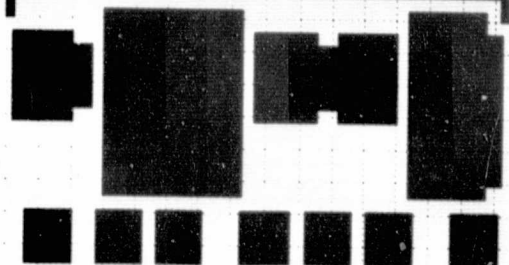
PIN	CAPACITANCE (pF)	
	Non-Transmitting	Transmitting
2	1.57	1.57
3	1.69	577 + Ext C
4	4.08	"
5	1.69	5.77 + C Ext
6	1.57	1.57
7	1.69	5.77 + C Ext
8	1.57	1.57



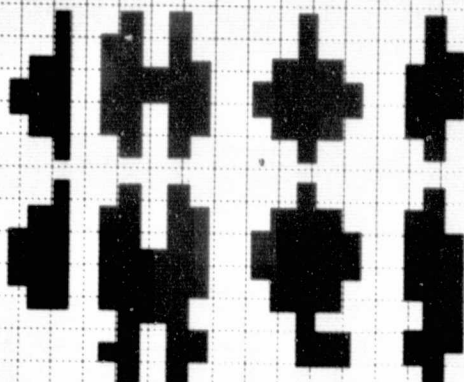


LEV 1

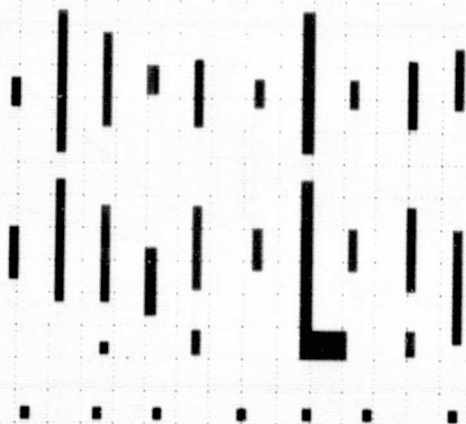
LEV 2



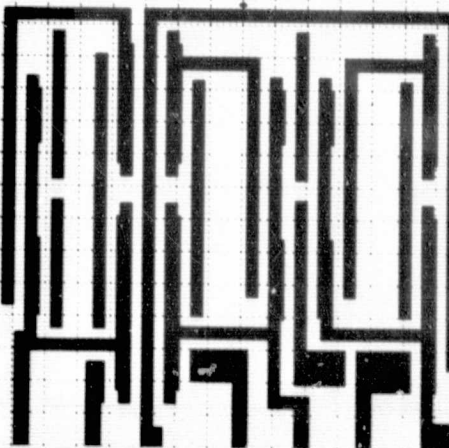
LEV 3



LEV 4



LEV 5



LEV 6

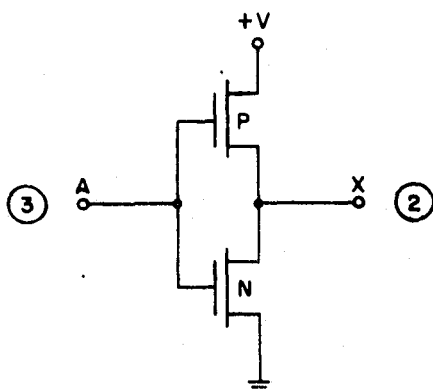
DOUBLE BUFFER INVERTER

2 Devices
2 Pads

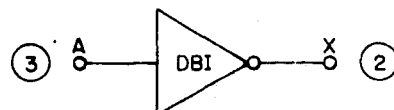
Cell Width = 3.9 mils

C-MOS STANDARD
CELL NO. 1520

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

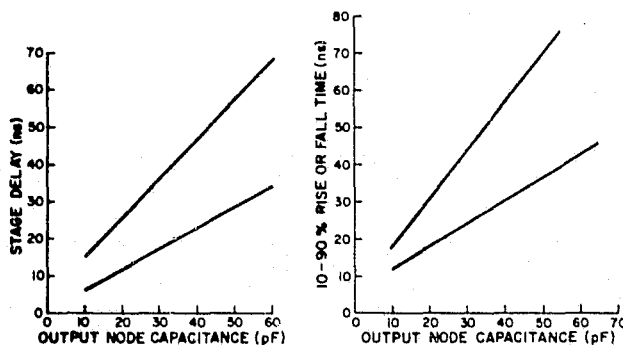
$$X = \overline{A}$$

TRUTH TABLE

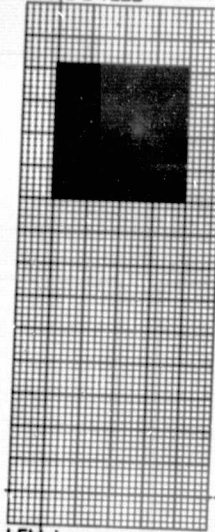
A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES

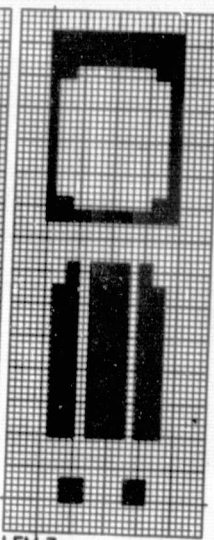
PIN	CAPACITANCE (pF)
2	1.79
3	3.94



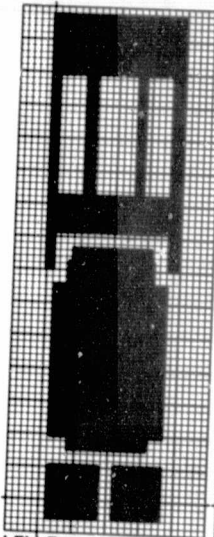
MSFC C 1520



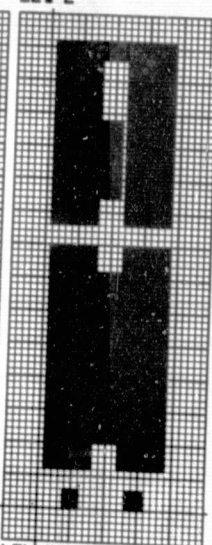
LEV 1



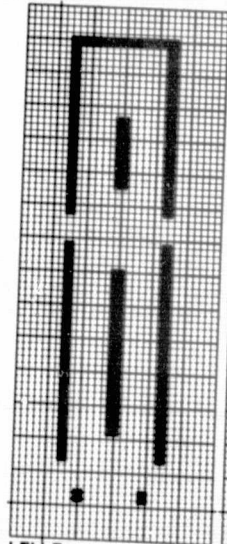
LEV 2



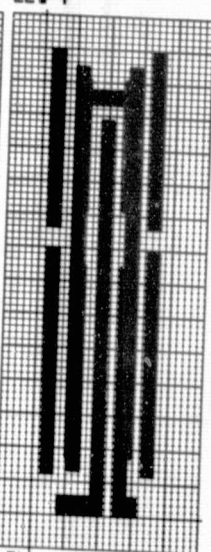
LEV 3



LEV 4



LEV 5



LEV 6

ORIGINAL PAGE IS
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DOUBLE BUFFER/BUFFER/INVERTER

4 Devices

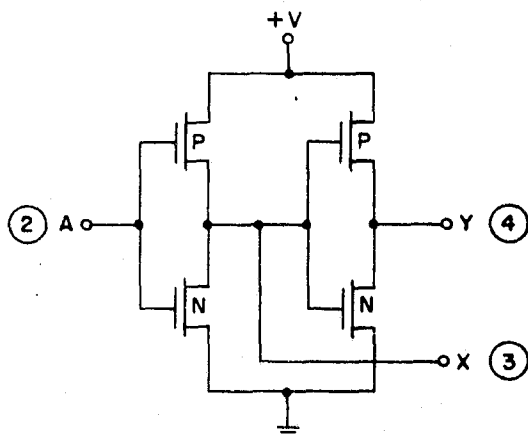
3 Pads

Cell Width = 5.8 mils

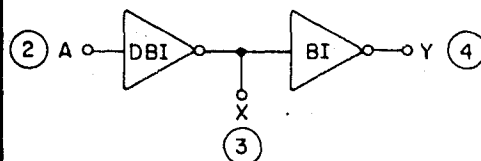
C-MOS STANDARD

CELL NO. 1530

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

$$X = \bar{A}$$

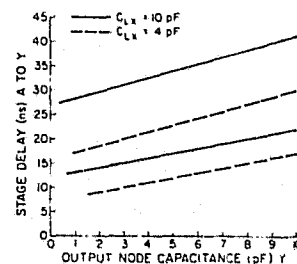
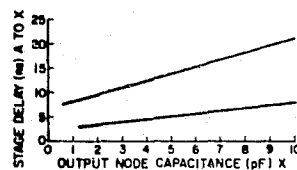
$$Y = A$$

TRUTH TABLE

A	X	Y
0	1	0
1	0	1

CELL I/O CAPACITANCE VALUES

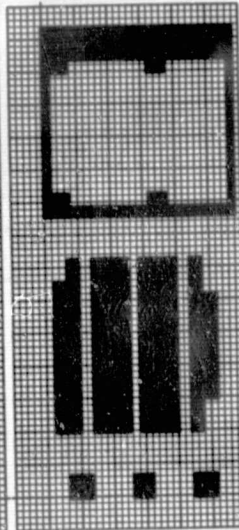
PIN	CAPACITANCE (pF)
2	3.94
3	3.55
4	1.21



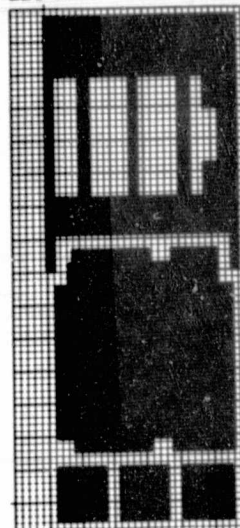
MSFC C 1530



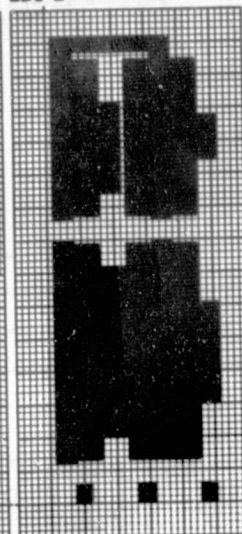
LEV 1



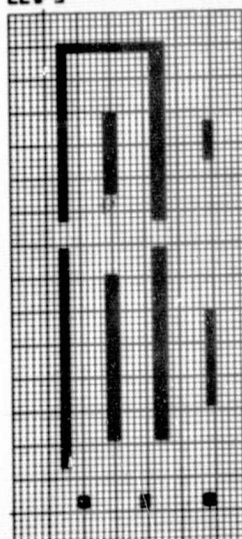
LEV 2



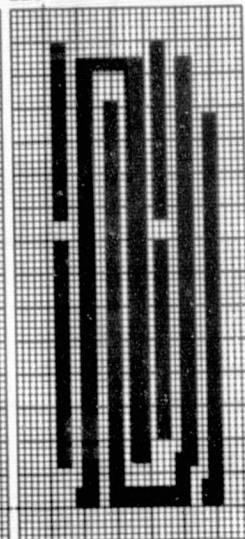
LEV 3



LEV 4



LEV 5



LEV b

ORIGINAL PAGE IS
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2 INPUT AND GATE

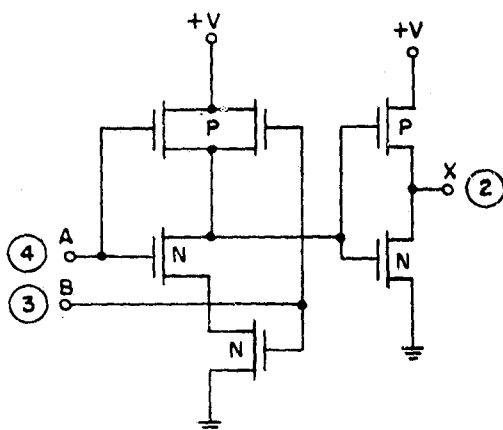
6 Devices

3 Pads

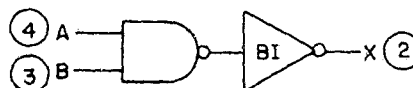
Cell Width = 5.8 mils

C-MOS STANDARD
CELL NO. 1620

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

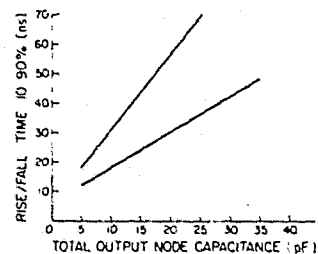
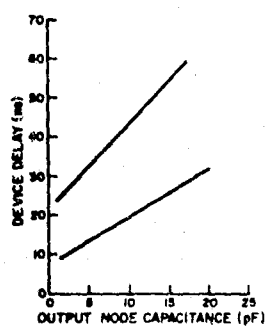
$$X = A \cdot B$$

TRUTH TABLE

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

CELL I/O CAPACITANCE VALUES

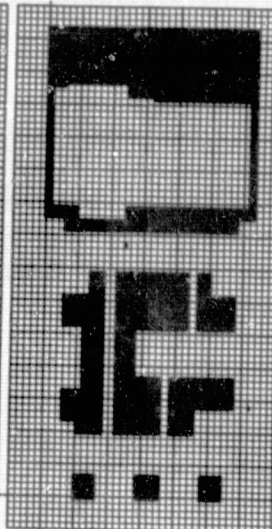
PIN	CAPACITANCE (pF)
2	1.21
3	1.17
4	1.17



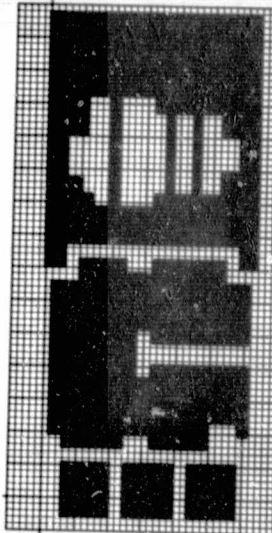
MSFC C 1620



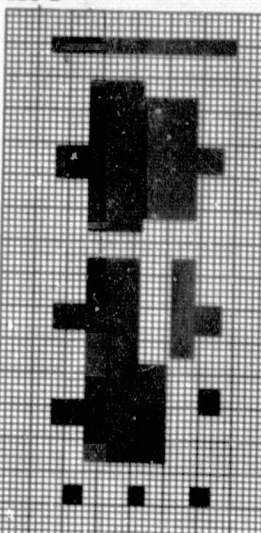
LEV 1



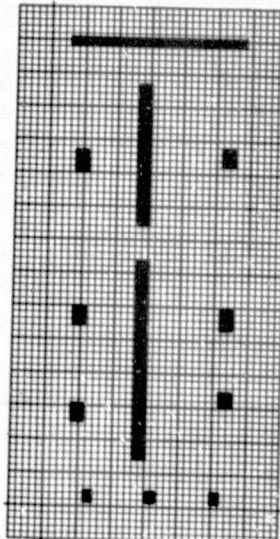
LEV 2



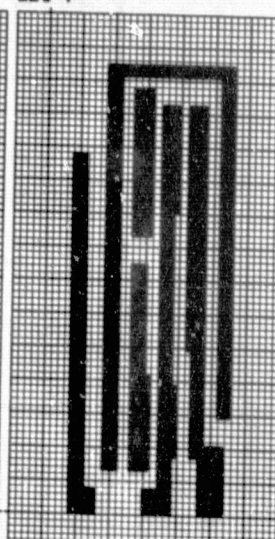
LEV 3



LEV 4



LEV 5



LEV 6

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3 INPUT AND GATE

8 Devices

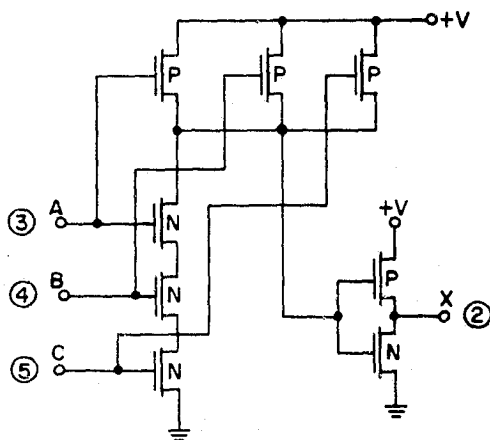
4 Pads

C-MOS STANDARD CELL

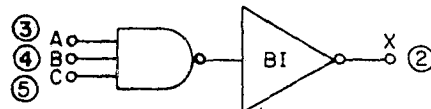
CELL NO. 1630

Cell Width = 7.7 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

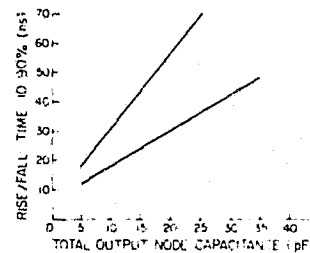
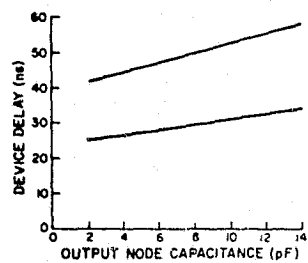
$$X = ABC$$

TRUTH TABLE

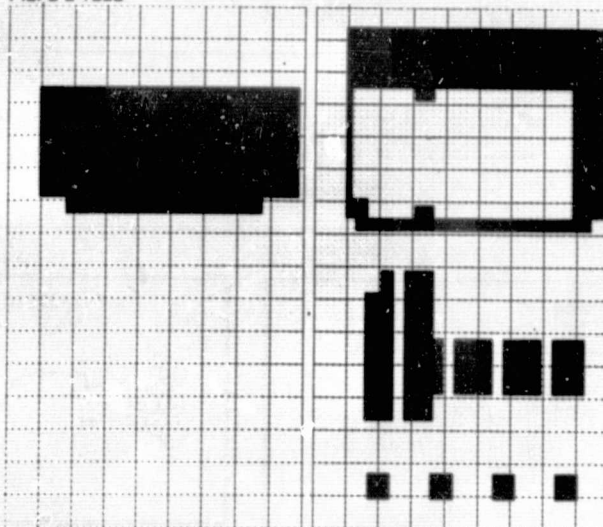
A	B	C	X
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
1	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.21
3	1.40
4	1.40
5	1.40

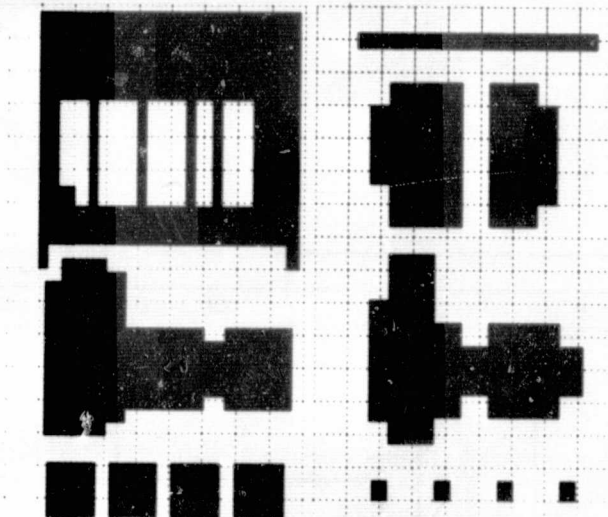


MSFC C 1630



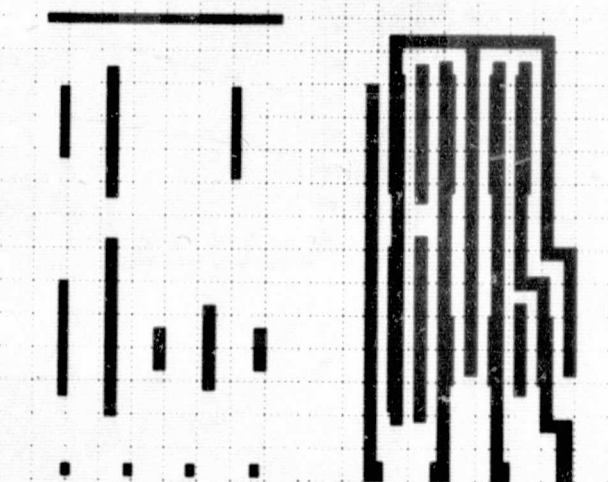
LEV 1

LEV 2



LEV 3

LEV 4



LEV 5

LEV 6

ORIGINAL PAGE IS
OF POOR QUALITY

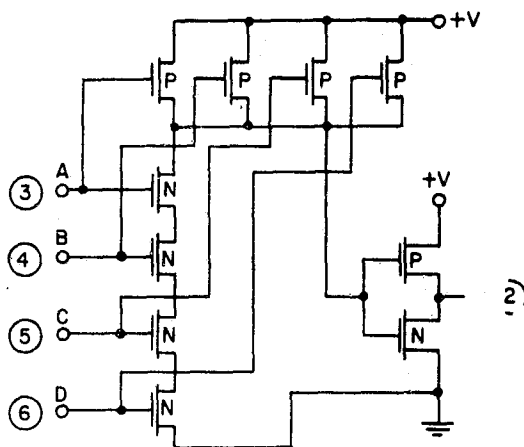
4 INPUT AND GATE

10 Devices
5 Pads

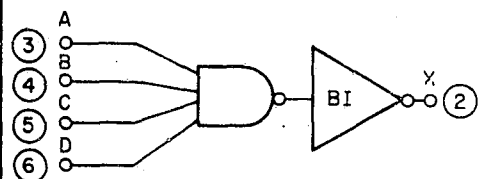
Cell Width = 9.6 mils

C-MOS STANDARD
CELL NO. 1640

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

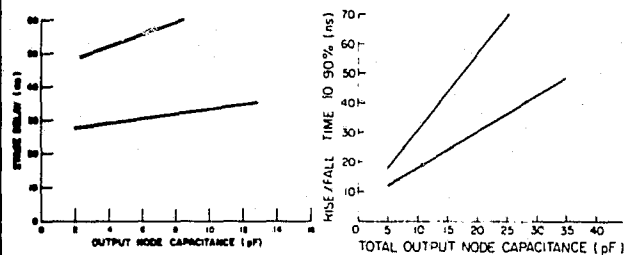
$$X = ABCD$$

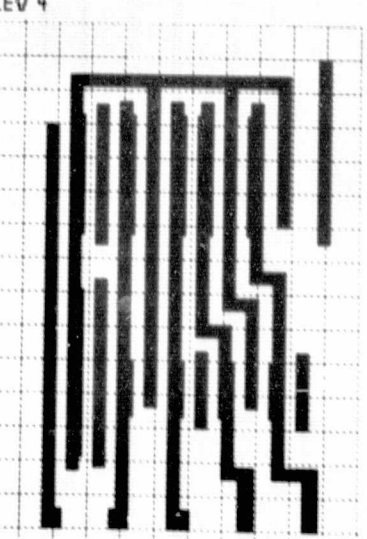
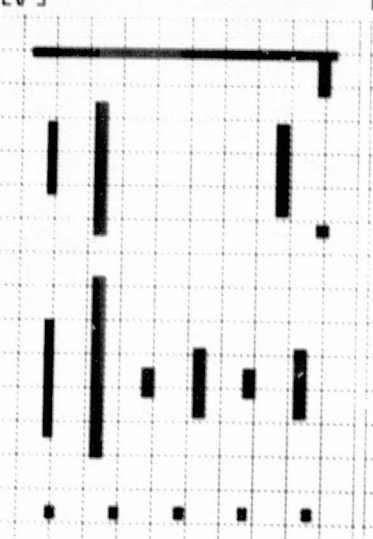
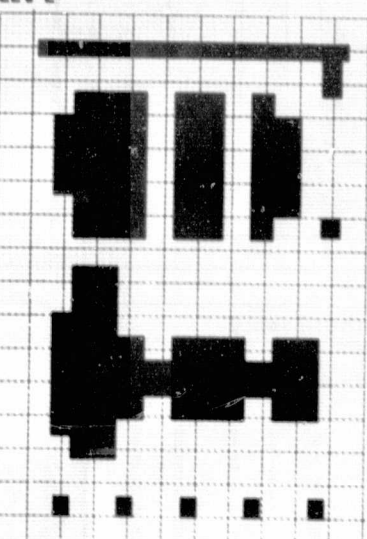
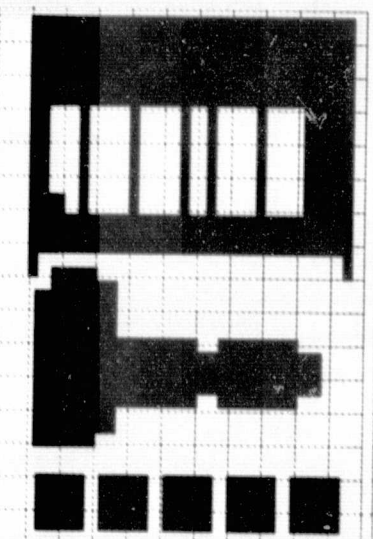
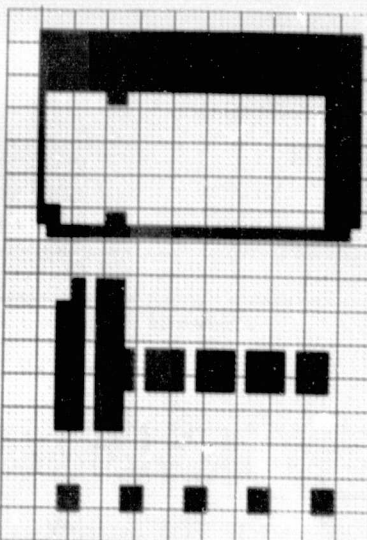
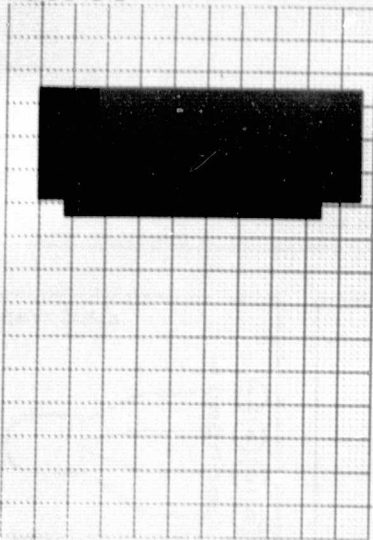
TRUTH TABLE

A	B	C	D	X
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.21
3	1.30
4	1.30
5	1.30
6	1.30





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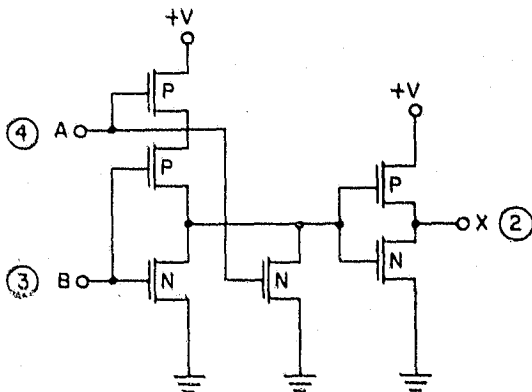
2 INPUT OR GATE

6 Devices
3 Pads

Cell Width = 5.8 mils

C-MOS STANDARD
CELL NO. 1720

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

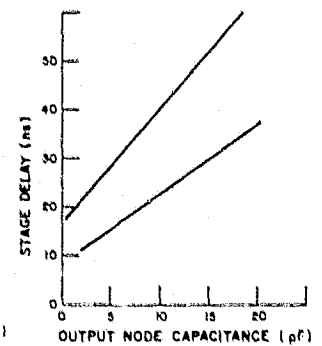
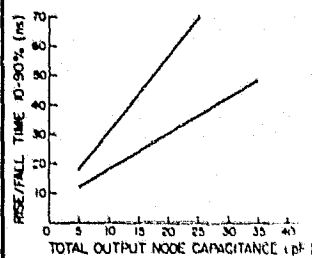
$$X = A + B$$

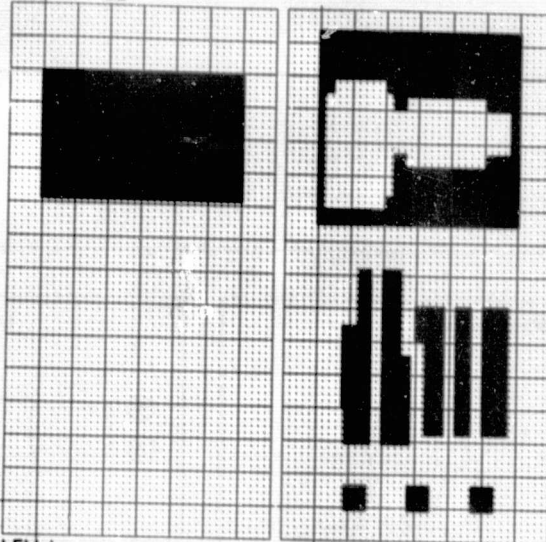
TRUTH TABLE

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

CELL I/O CAPACITANCE VALUES

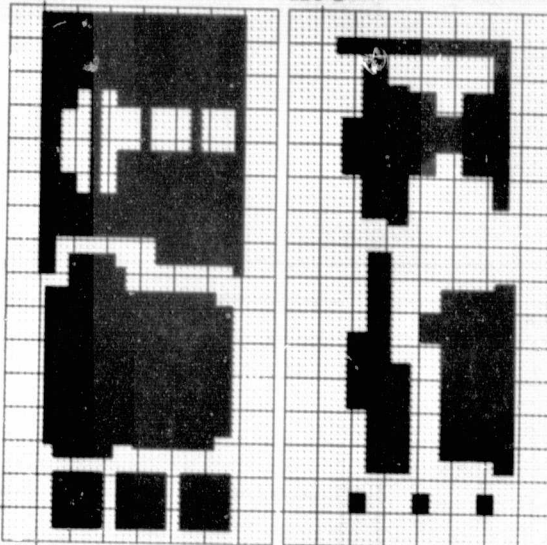
PIN	CAPACITANCE (pF)
2	1.21
3	1.30
4	1.30





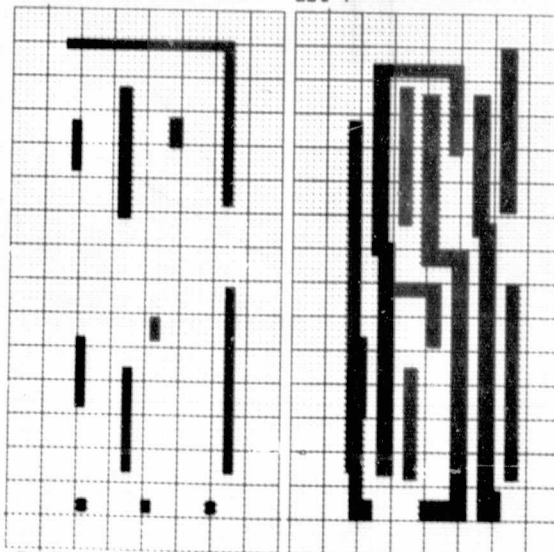
LEV 1

LEV 2



LEV 3

LEV 4



LEV 5

LEV 6

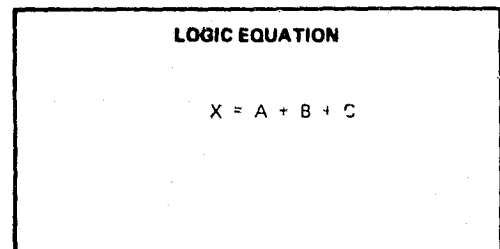
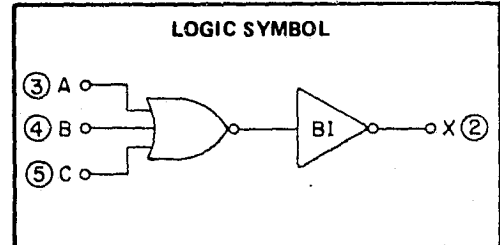
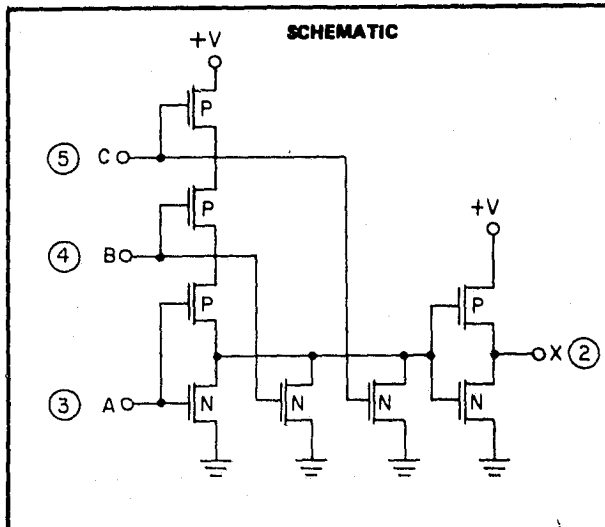
ORIGINAL PAGE IS
OF POOR QUALITY

3 INPUT OR GATE

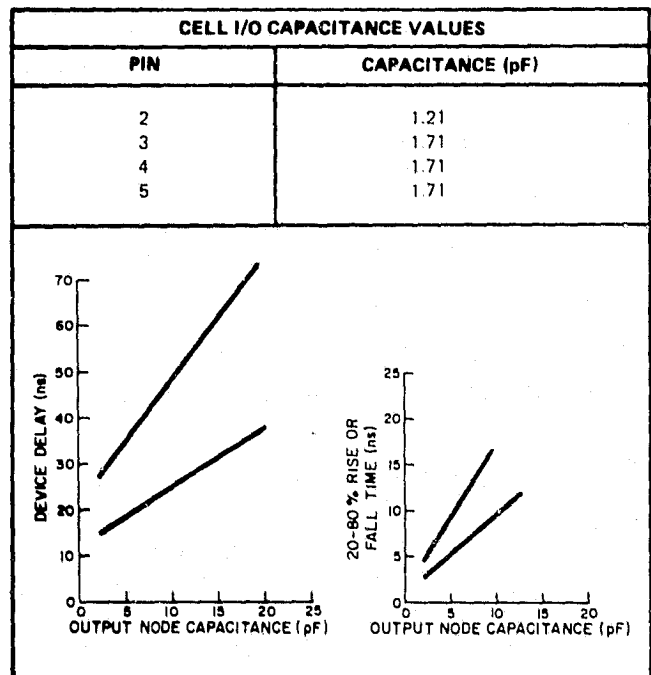
8 Devices
4 Pads

Cell Width = 7.7 mils

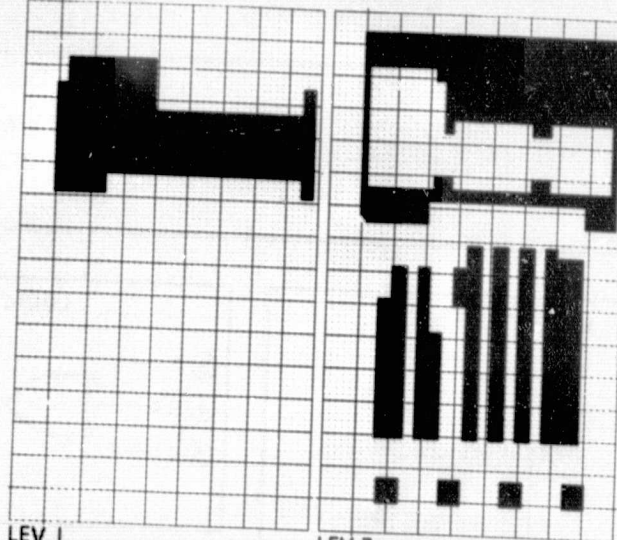
C-MOS STANDARD
CELL NO. 1730



TRUTH TABLE			
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	1

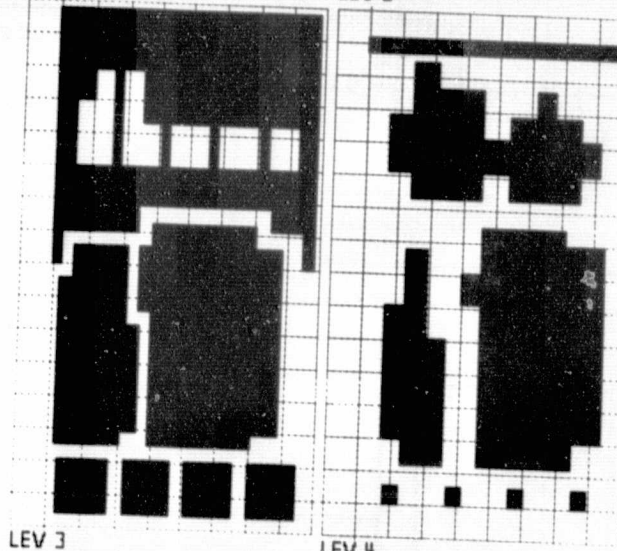


MSFC C 1730



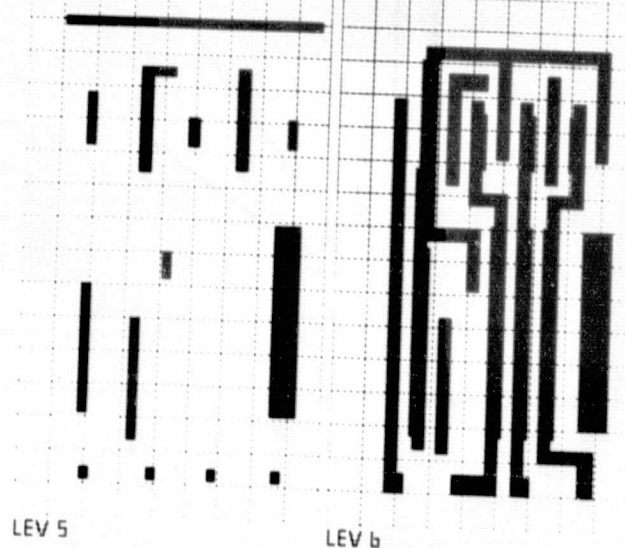
LEV 1

LEV 2



LEV 3

LEV 4



LEV 5

LEV 6

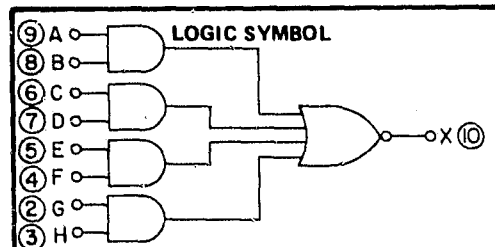
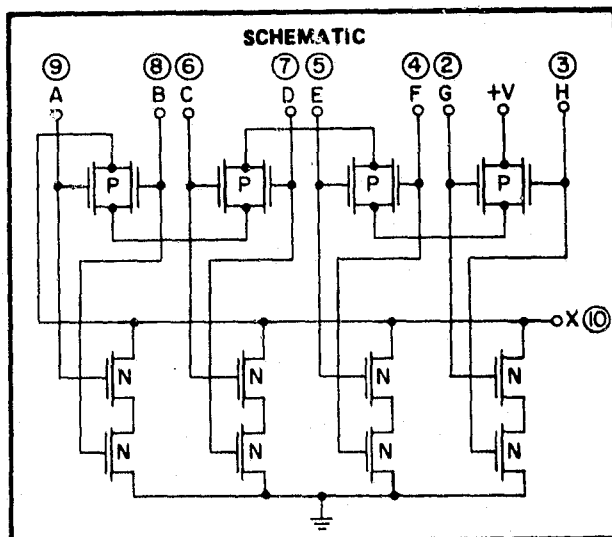
ORIGINAL PAGE IS
OF POOR QUALITY

4 X 2 INPUT AND +4 X NOR GATE

16 Devices
9 Pads

Cell Width = 17.2 mils

C-MOS STANDARD CELL CELL NO. 1800



LOGIC EQUATION

$$(AB + CD + EF + GH) = X$$

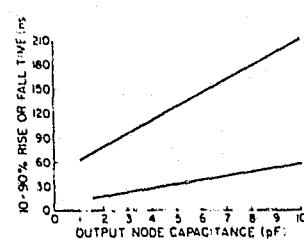
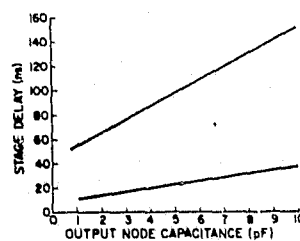
TRUTH TABLE

A	B	C	D	E	F	G	H	X
1	1	0
.	.	1	1	0
.	.	.	.	1	1	.	.	0
.	1	1	0
All other input combinations								1

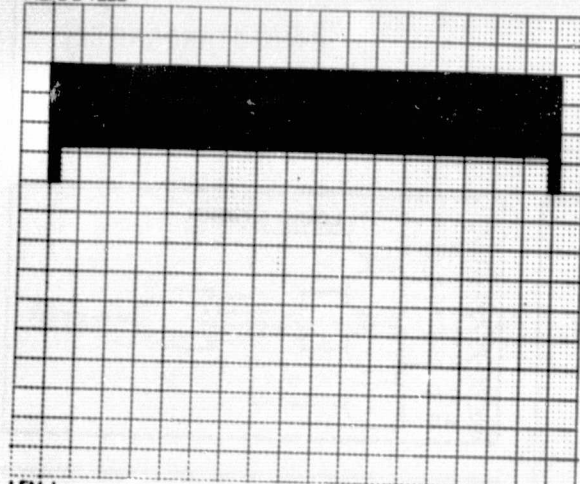
* either "1" or "0"

CELL I/O CAPACITANCE VALUES

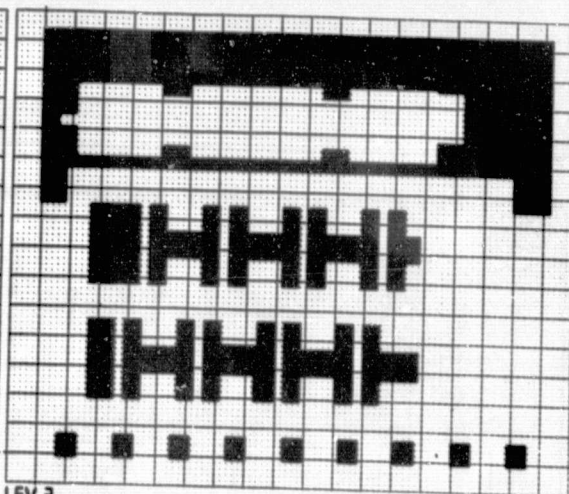
PIN	CAPACITANCE (pF)
2	1.27
3	1.00
4	1.39
5	1.60
6	1.60
7	1.38
8	1.36
9	1.60
10	2.18



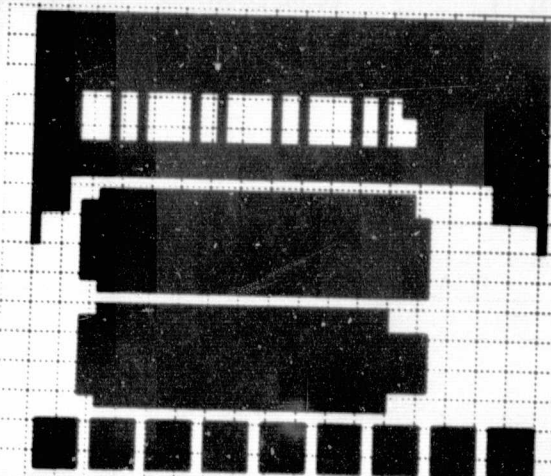
MSFC C 1800



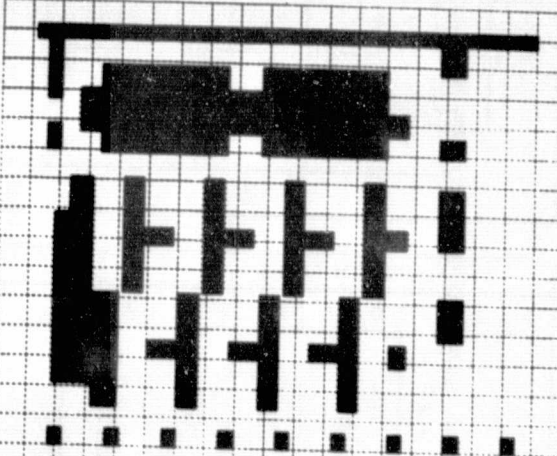
LEV 1



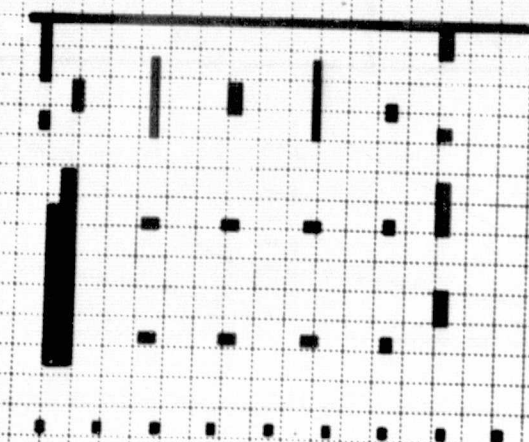
LEV 2



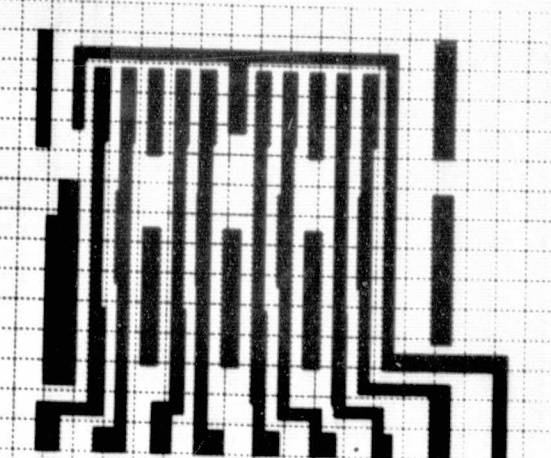
LEV 3



LEV 4



LEV 5



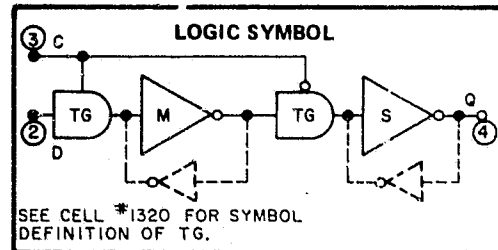
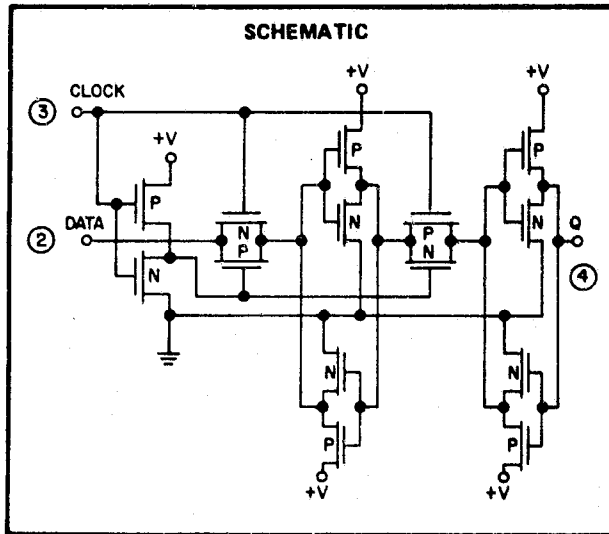
LEV 6

M/S FLIP-FLOP

14 Devices
3 Pads

Cell Width = 8.5 mils

C-MOS STANDARD
CELL NO. 1820



CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.50
3	1.00
4	0.67

TRUTH TABLE

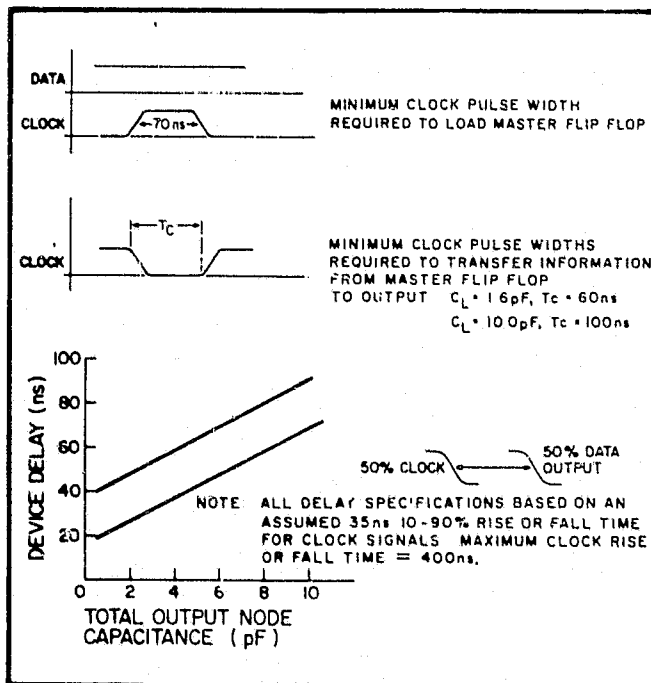
C	D	Q_n
1	1	1
1	0	0
0	1	Q_{n-1}
0	0	Q_{n-1}

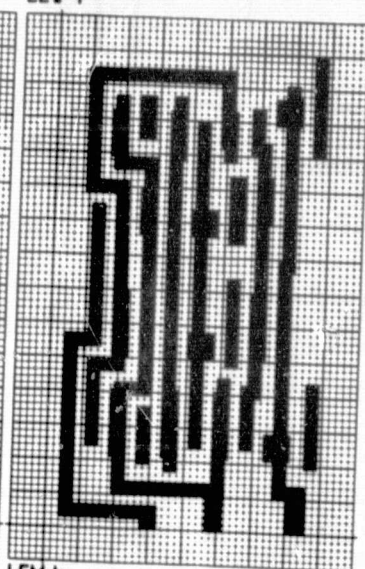
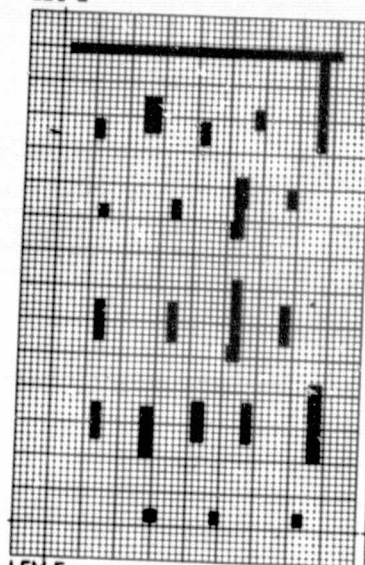
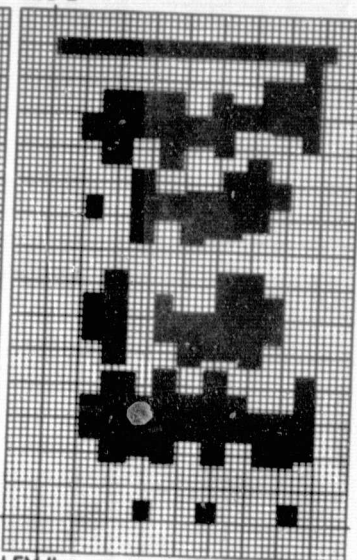
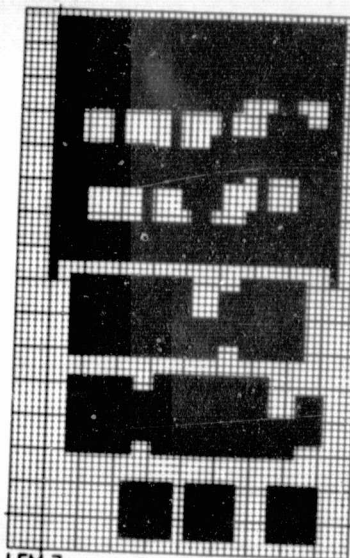
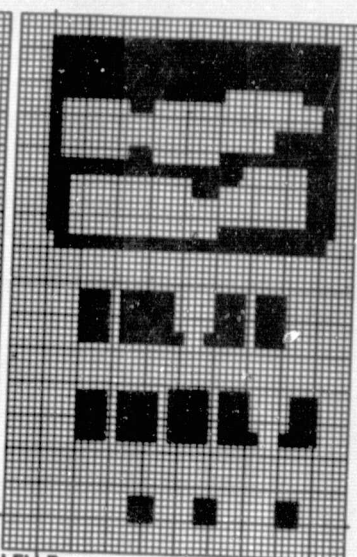
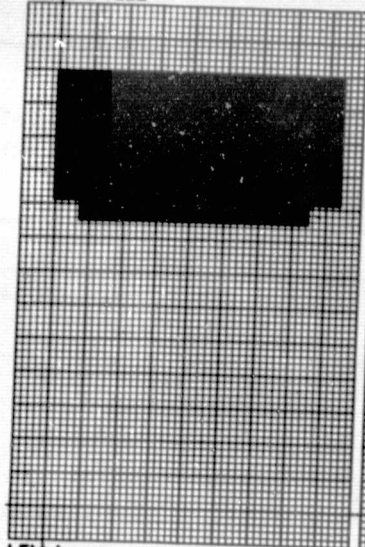
Q_{n-1} is output before clock goes high

LOGIC EQUATION

$$Q_n = Q_{n-1}C + D_{n-1}\bar{C}$$

D_{n-1} } Are input & output respectively
 Q_{n-1} } before clock changes state





ORIGINAL PAGE IS
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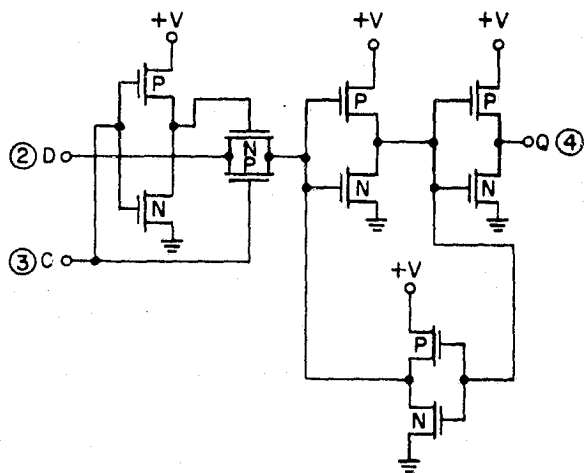
D-TYPE FLIP FLOP

10 Devices
3 Pads

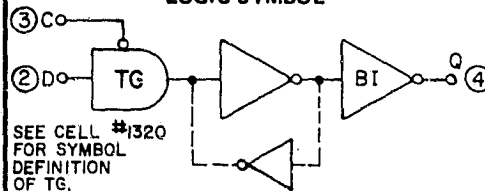
Cell Width = 8.4 mils

C-MOS STANDARD CELL
CELL NO. 1830

SCHEMATIC



LOGIC SYMBOL



CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.70
3	1.46
4	1.40

TRUTH TABLE

D	C	Q
*	1	Q_{n-1}
1	0	1
0	0	0

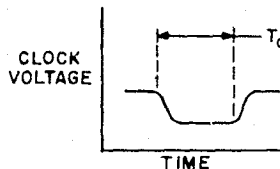
* can be either "0" or "1"

Q_{n-1} is output before clock goes high

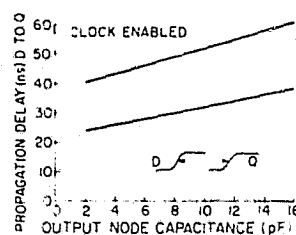
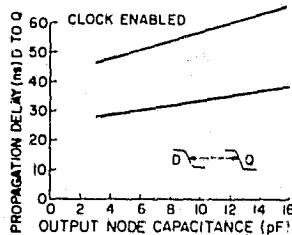
LOGIC EQUATION

$$Q = D \bar{C} + Q_{n-1} C$$

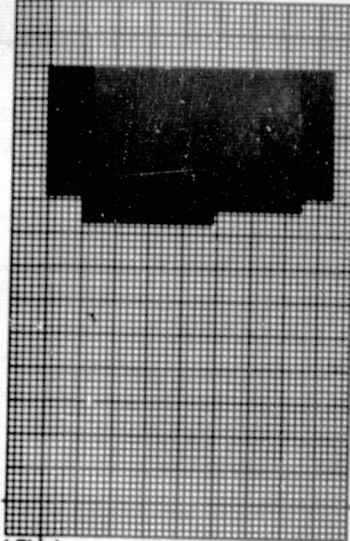
A is data, C is the clock, Q_{n-1} is Q before clock goes high.



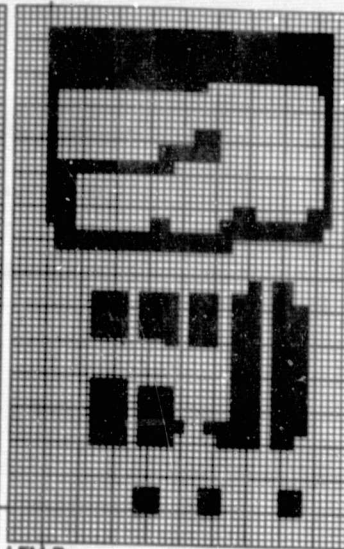
MINIMUM CLOCK PULSE WIDTH REQUIRED TO TRANSFER INFORMATION TO OUTPUT = 35 ns



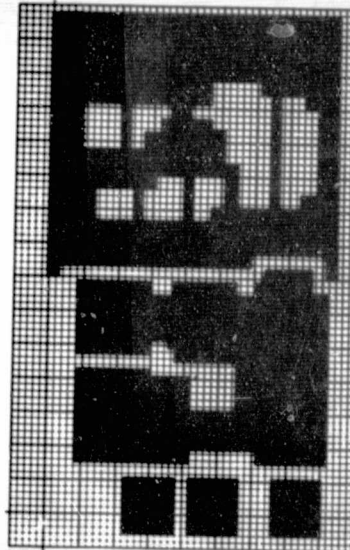
MSFC C 1830



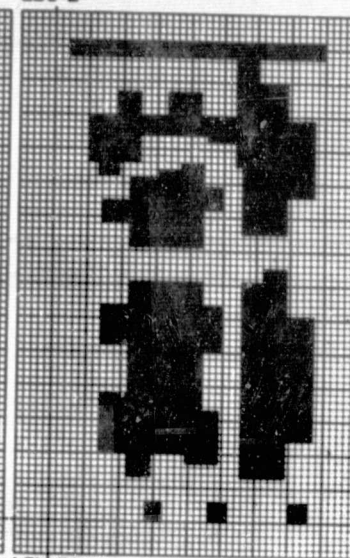
LEV 1



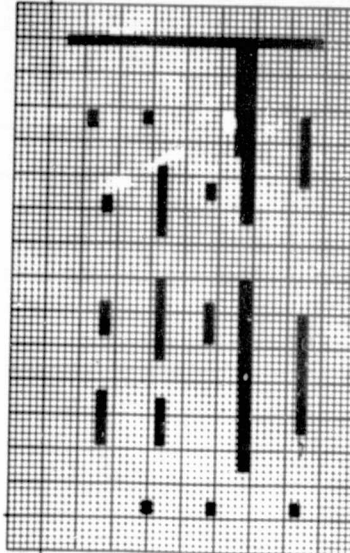
LEV 2



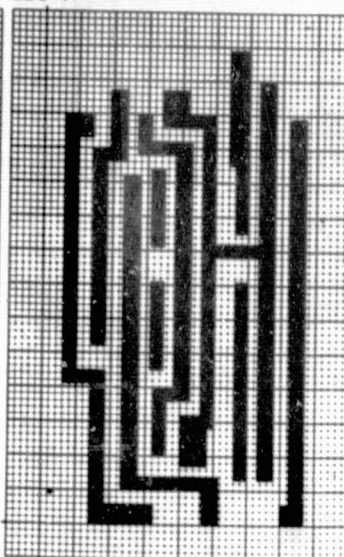
LEV 3



LEV 4



LEV 5



LEV 6

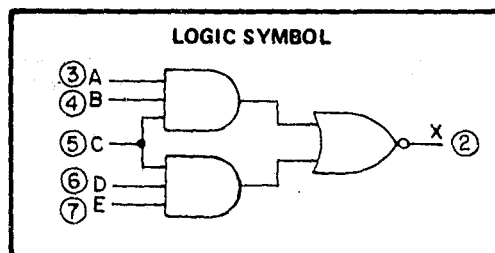
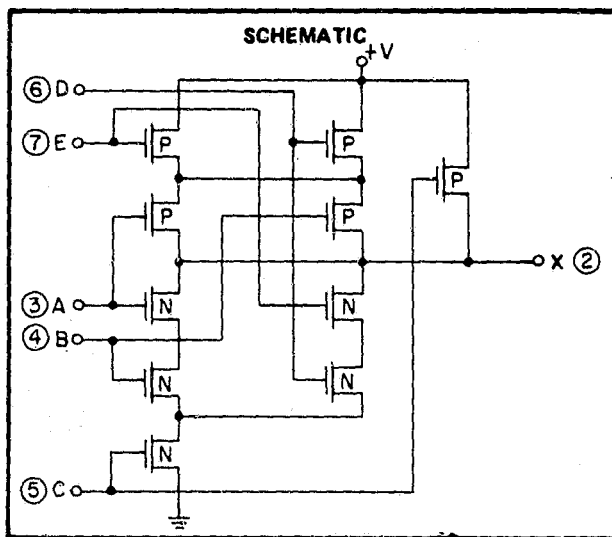
ORIGINAL PAGE IS
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1/2, 2 AND -2 NOR

10 Devices
6 Pads

Cell Width = 11.6 mils

C-MOS STANDARD CELL
CELL NO. 1840

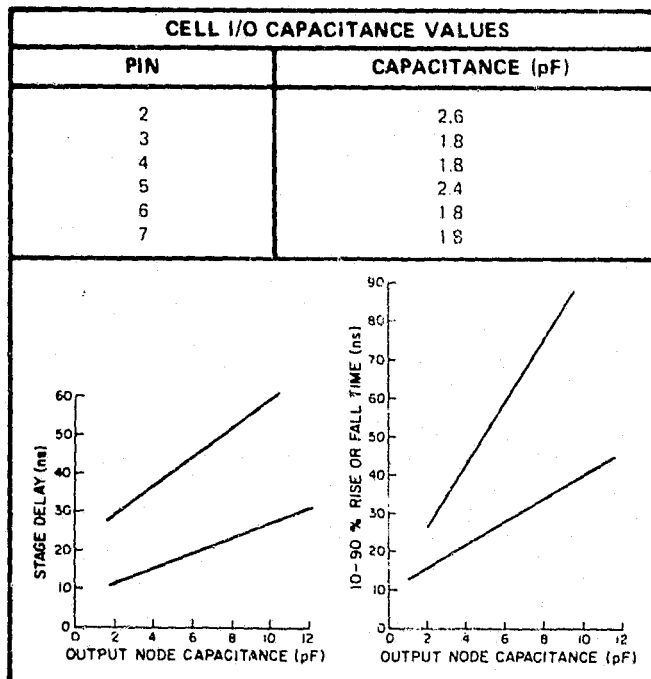


LOGIC EQUATION

$$X = \overline{C(AB + DE)}$$

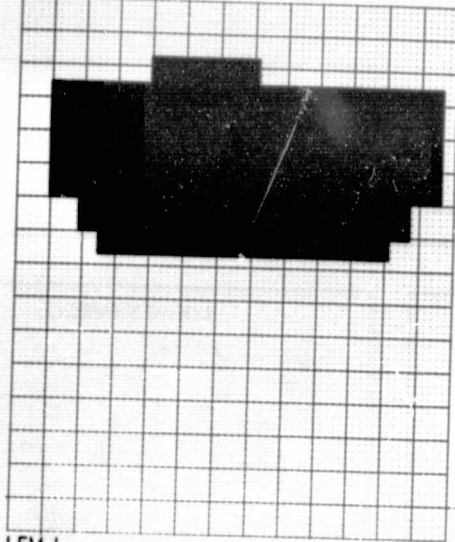
TRUTH TABLE					
	B	C	D	E	Z
1	1	1	.	.	0
.	.	1	1	1	0
All other input combinations					1

Don't Care

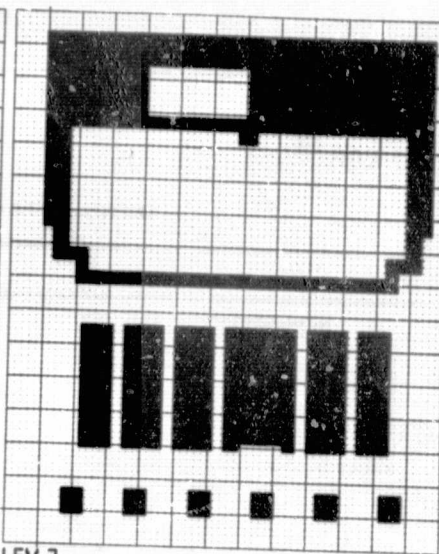


C-2

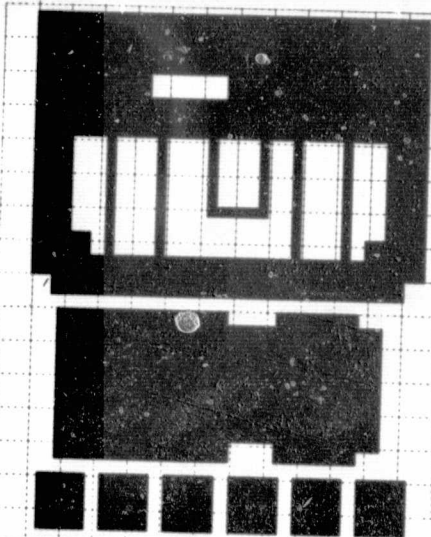
MSFC C 1840



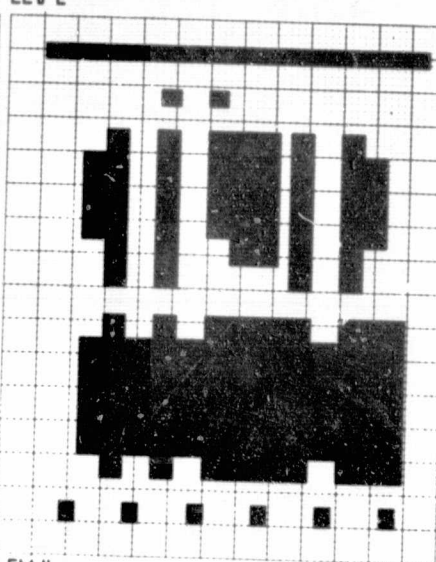
LEV 1



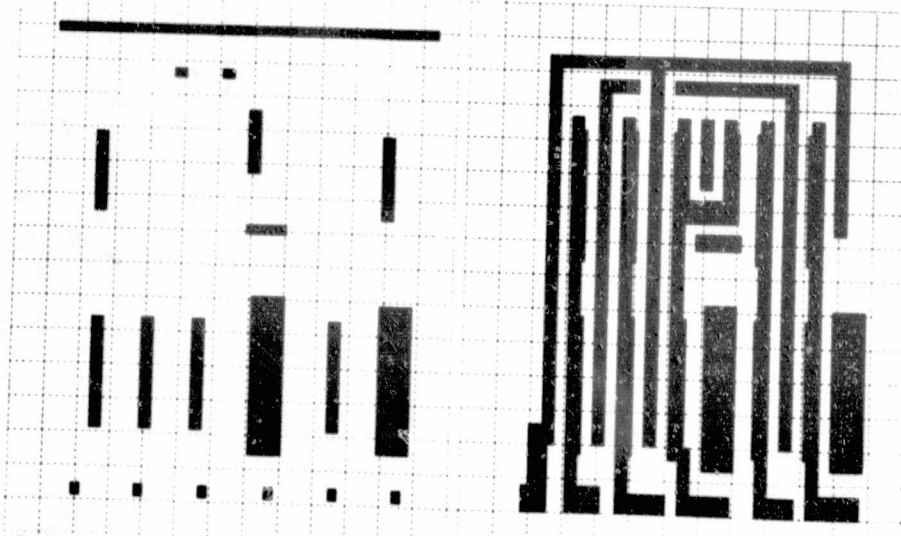
LEV 2



LEV 3



LEV 4



LEV 5

LEV 6

ORIGINAL PAGE IS
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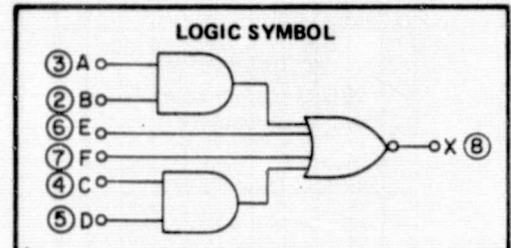
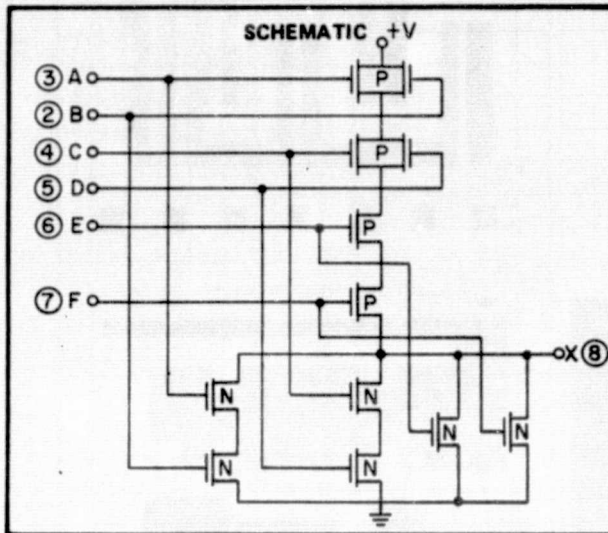
2, 2, AND -4 NOR

12 Devices

7 Pads

Cell Width = 13.7 mils

C-MOS STANDARD CELL
CELL NO. 1860

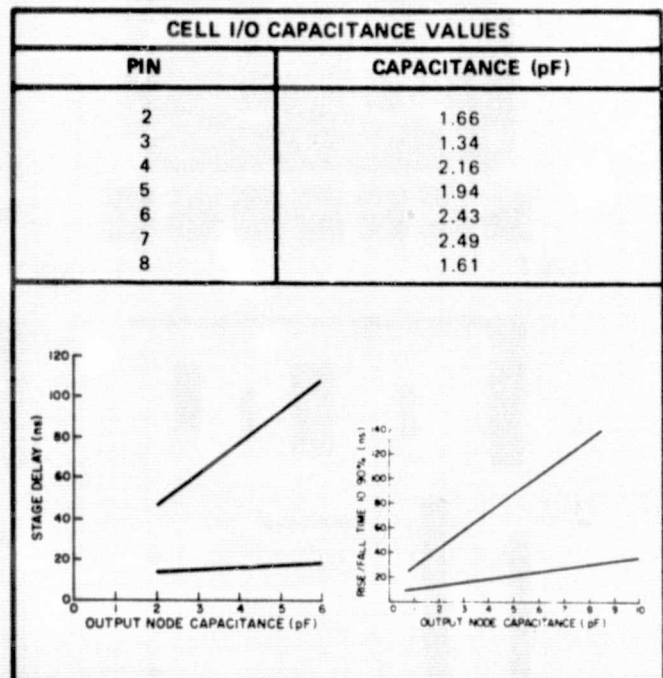


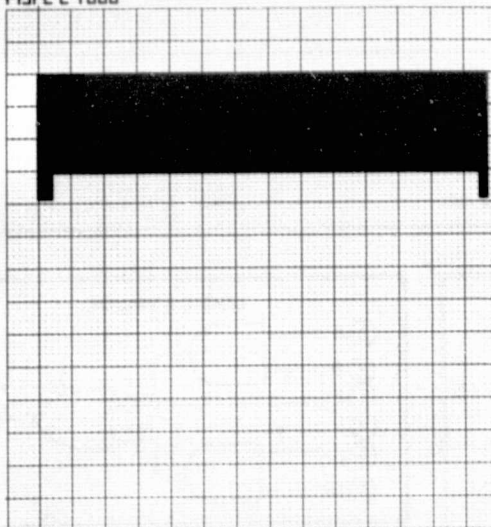
LOGIC EQUATION

$$X = \overline{(AB + E + F + CD)}$$

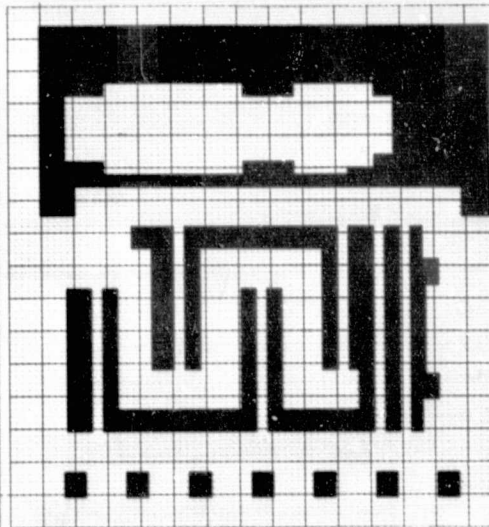
TRUTH TABLE						
A	B	C	D	E	F	G
1	1	*	*	*	*	0
*	*	*	*	1	*	0
*	*	*	*	*	1	0
*	*	1	1	*	*	0
All other input combinations						1

*Can be either "1" or "0"

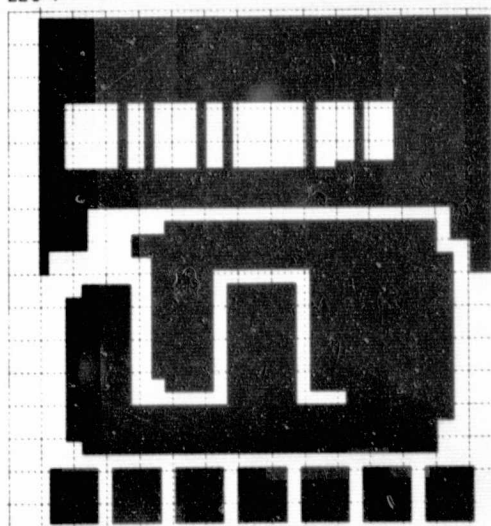




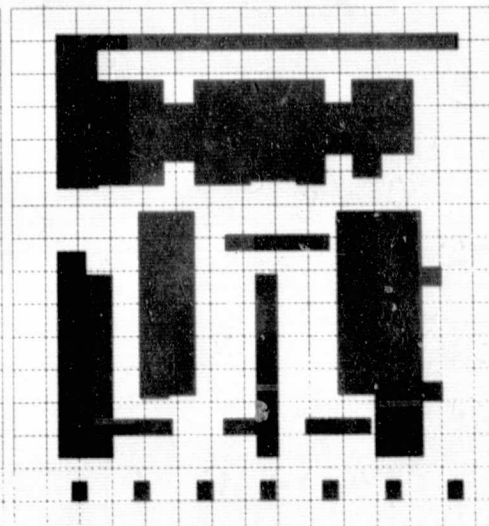
LEV 1



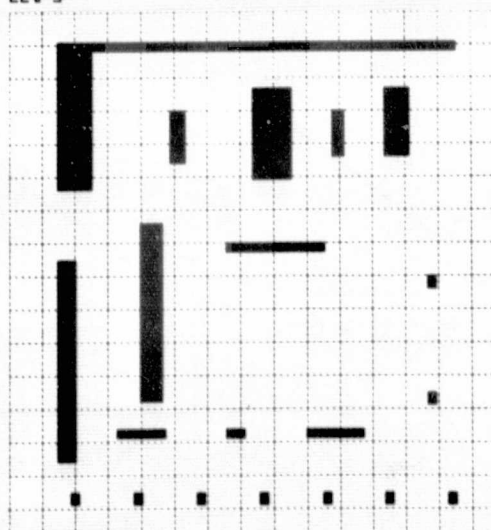
LEV 2



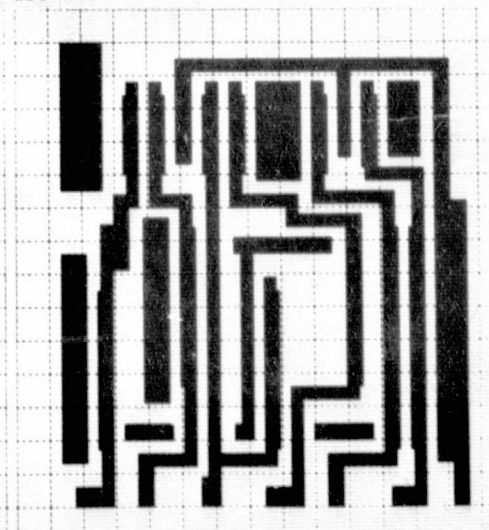
LEV 3



LEV 4



LEV 5



LEV 6

ORIGINAL PAGE IS
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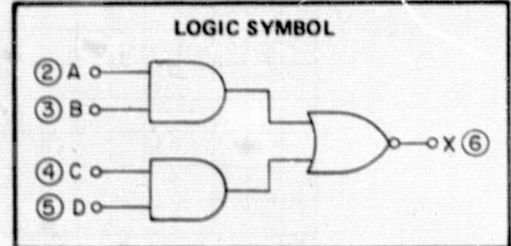
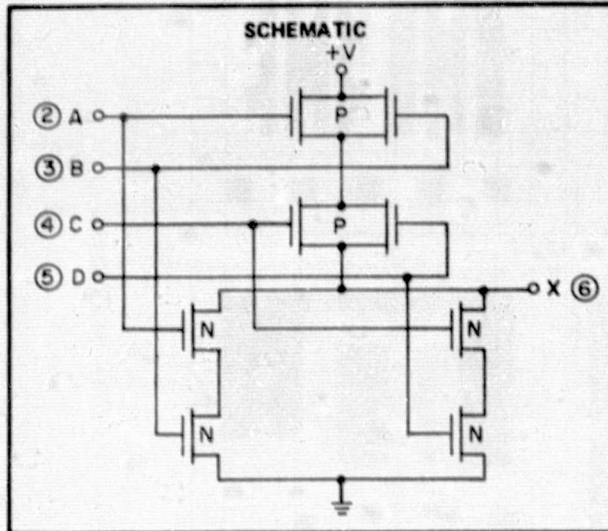
2, 2 AND -2 NOR

8 Devices

5 Pads

Cell Width = 9.6 mils

C-MOS STANDARD CELL
CELL NO. 1870

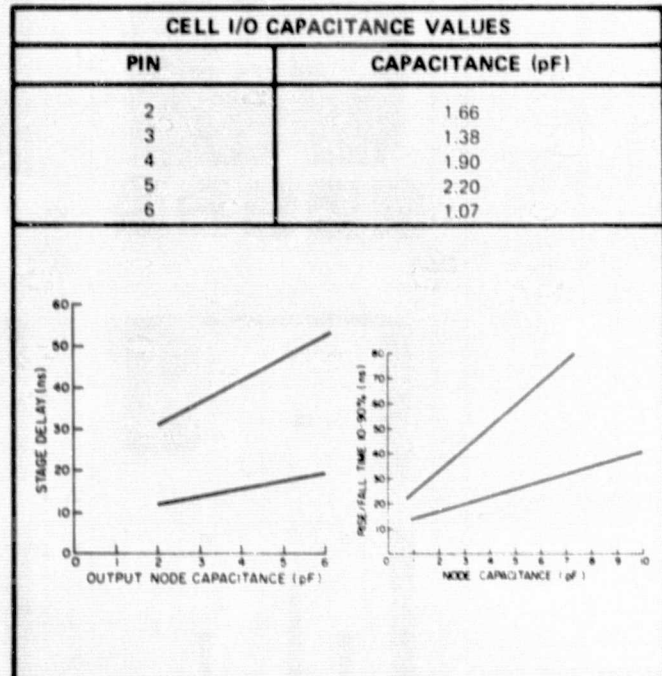


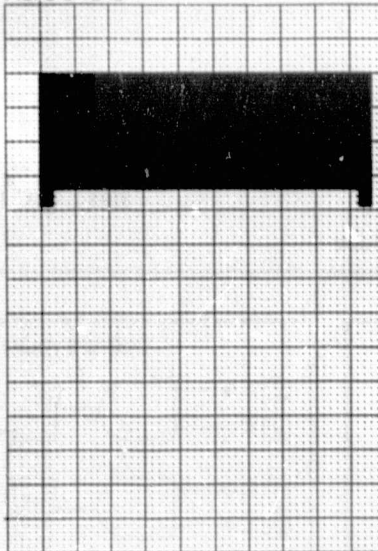
LOGIC EQUATION

$$X = \overline{(A \cdot B + C \cdot D)}$$

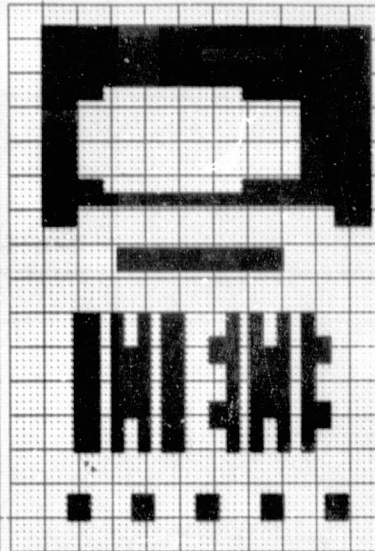
TRUTH TABLE				
A	B	C	D	X
1	1	*	*	0
0	*	1	1	0
All other input combinations				1

* can be either "1" or "0"

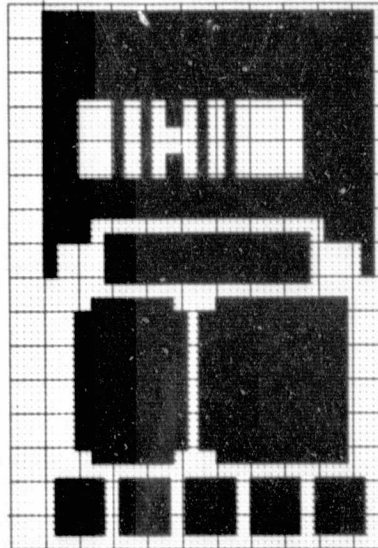




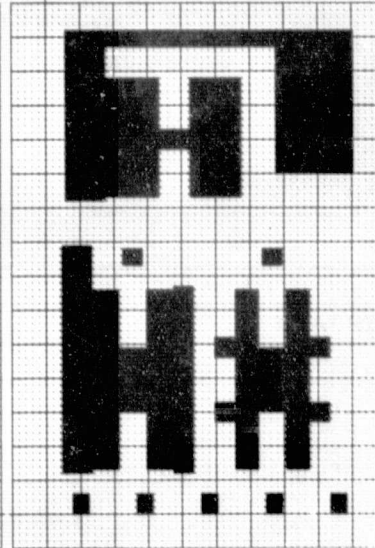
LEV 1



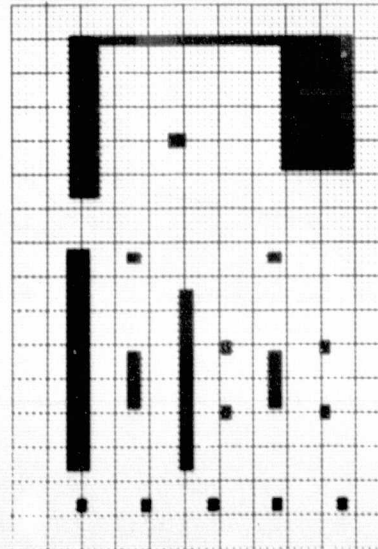
LEV 2



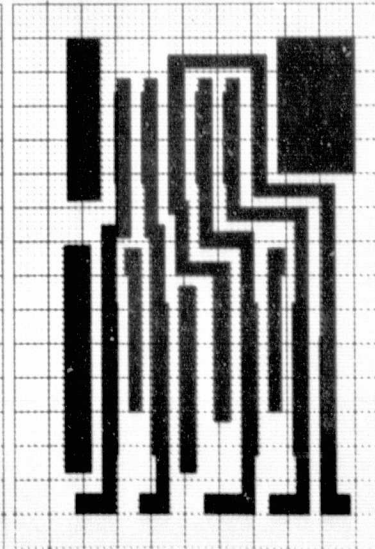
LEV 3



LEV 4



LEV 5



LEV b

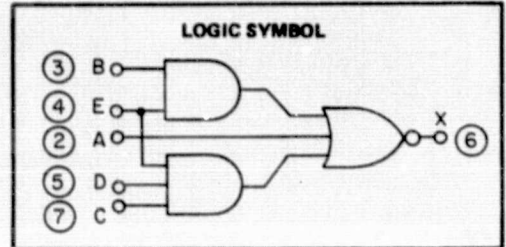
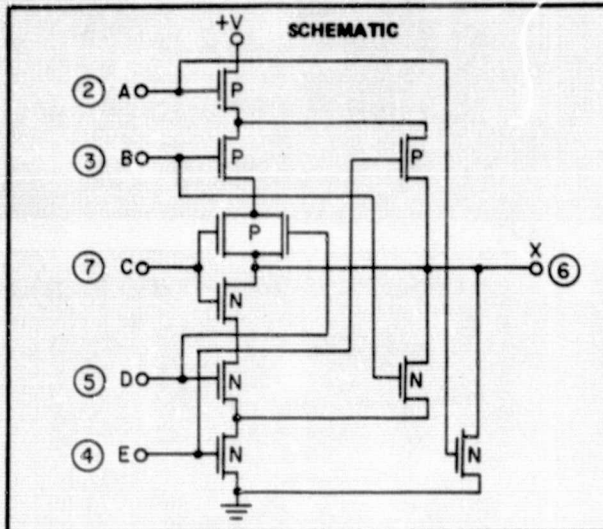
ORIGINAL PAGE IS
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2 BIT CARRY ANTICIPATE

10 Devices
7 Pads

Cell Length = 14.9 mils

C-MOS STANDARD
CELL NO. 1880

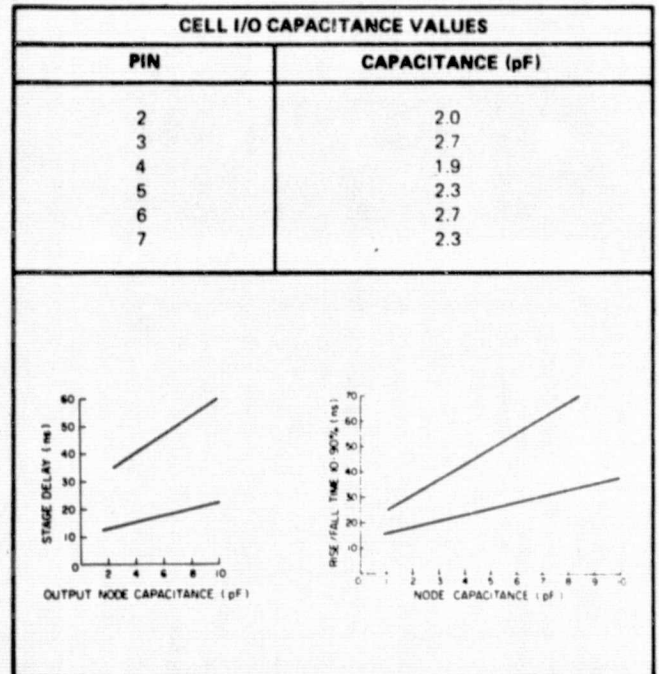


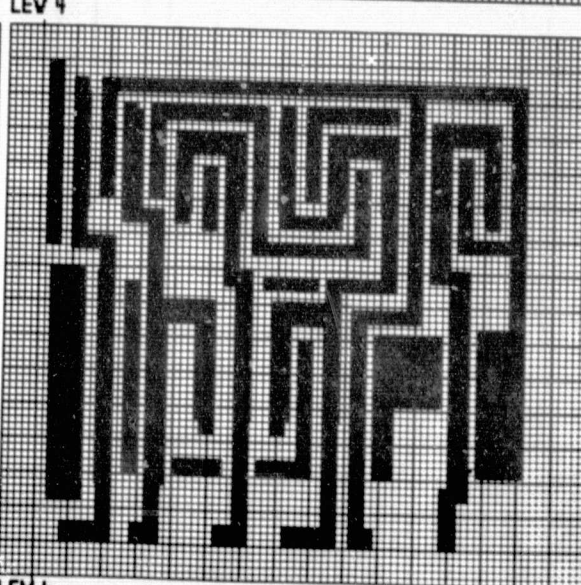
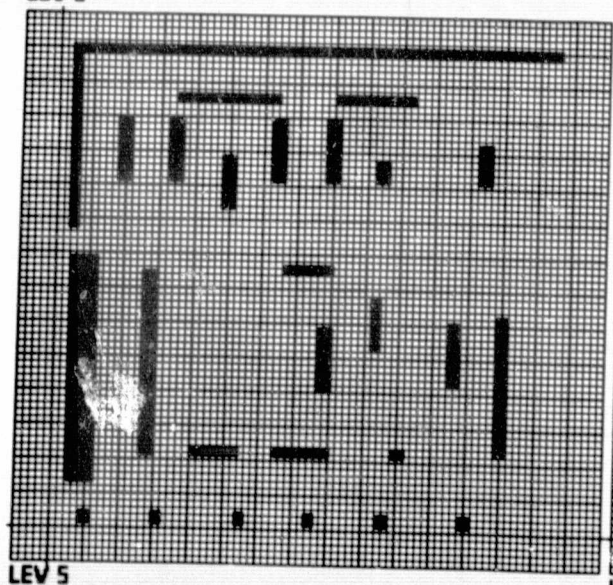
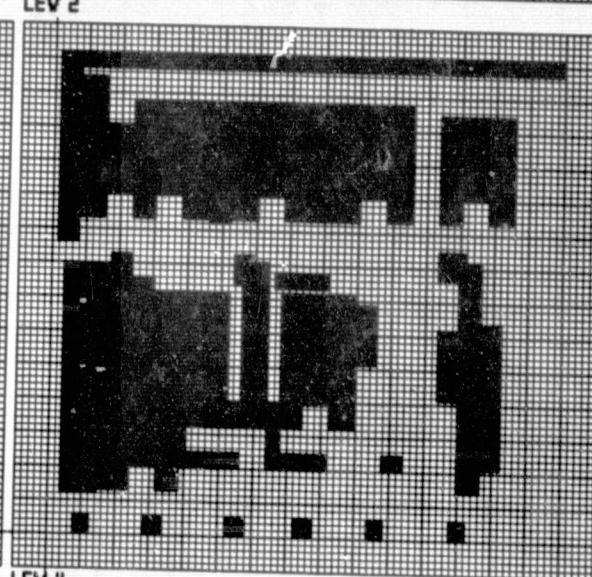
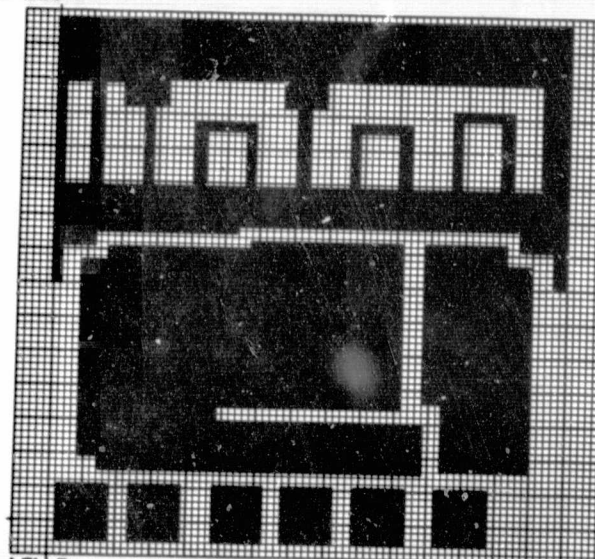
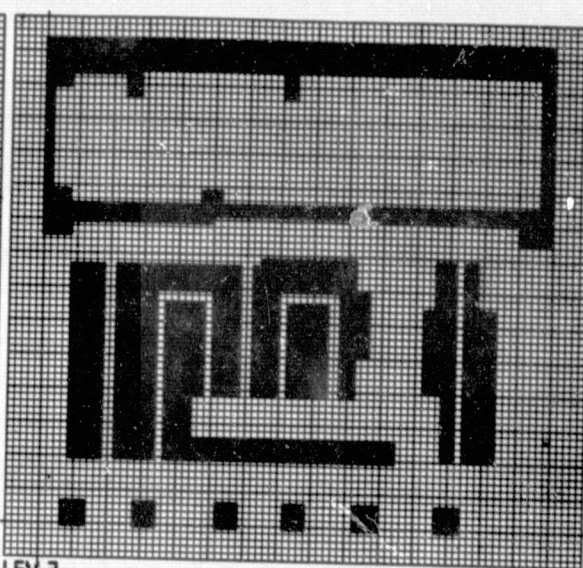
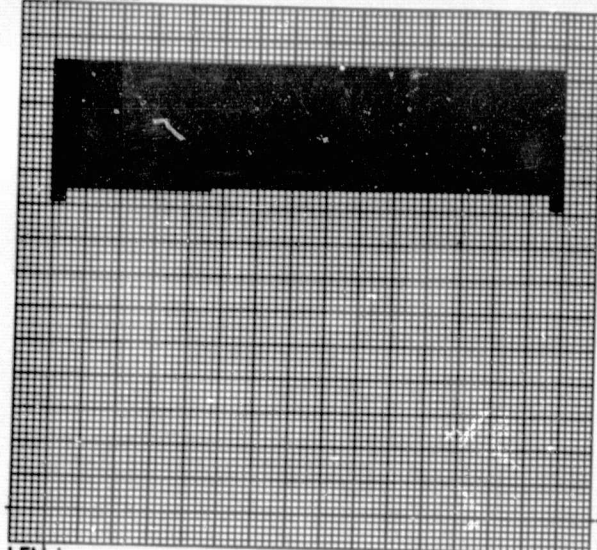
LOGIC EQUATION

$$X = \overline{(C \cdot D \cdot E) + (B \cdot E) + A}$$

TRUTH/TABLE					
B	A	D	E	C	X
*	1	*	*	*	0
1	*	*	1	*	0
*	*	1	1	1	0
ALL OTHER INPUT COMBINATIONS					1

*Can be either "1" or "0"



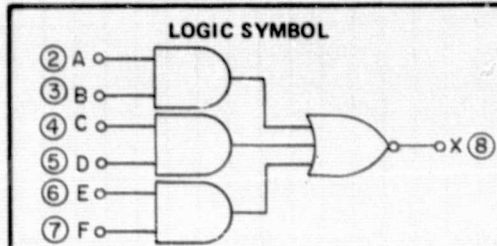
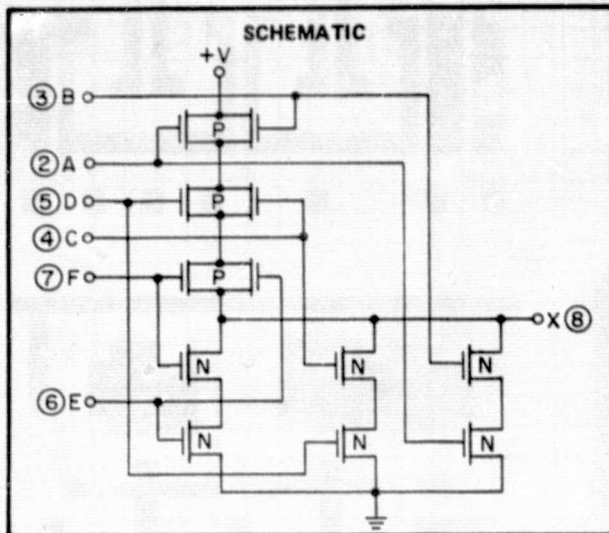


2,2,2 AND -3 NOR

12 Devices
7 Pads

Cell Width = 16.9 mils

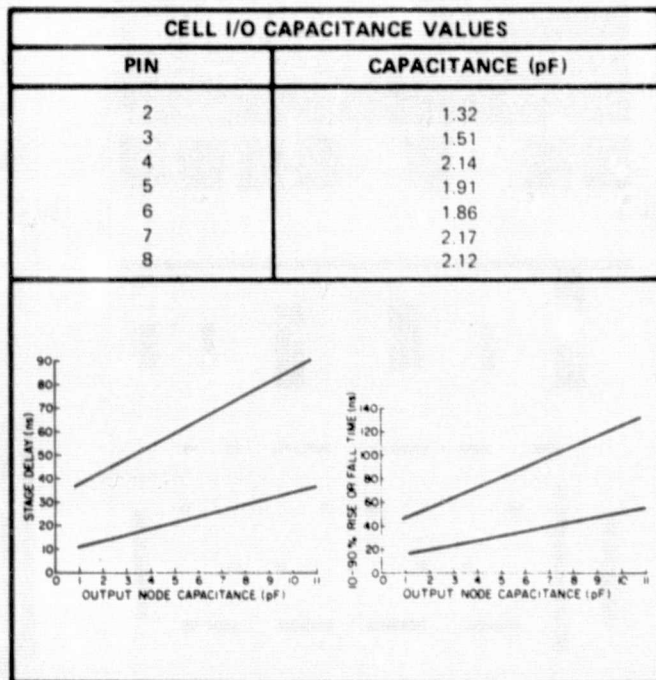
C-MOS STANDARD CELL
CELL NO. 1890

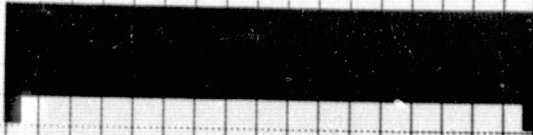


LOGIC EQUATION

$$X = \overline{(AB + CD + EF)}$$

TRUTH TABLE						
A	B	C	D	E	F	X
1	1	*	*	*	*	0
*	*	1	1	*	*	0
*	*	*	*	1	1	0
All other input combinations						1

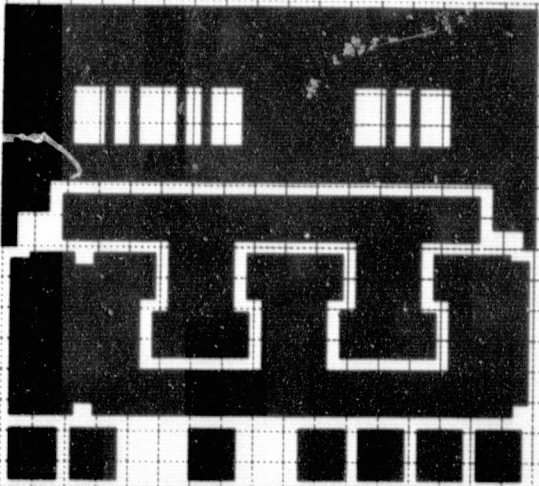




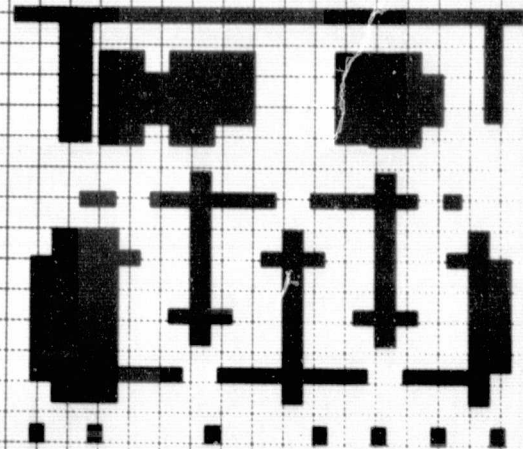
LEV 1



LEV 2



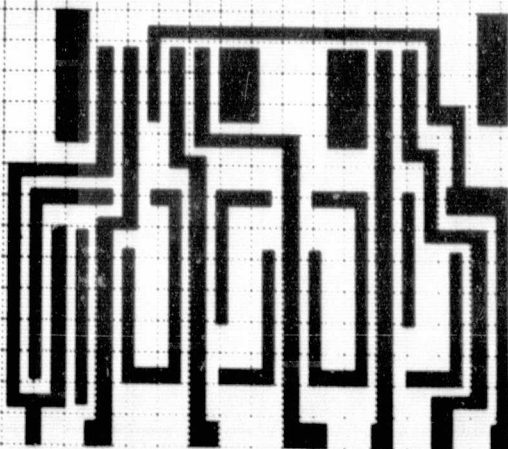
LEV 3



LEV 4



LEV 5



LEV 6

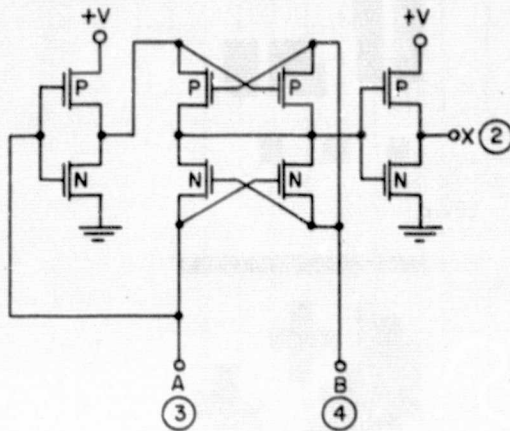
EOR – EXCLUSIVE OR

8 Devices
3 Pads

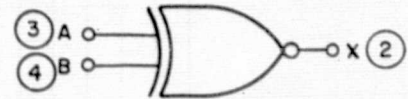
Cell Width = 7.8 mils

C-MOS STANDARD CELL
CELL NO. 2310

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

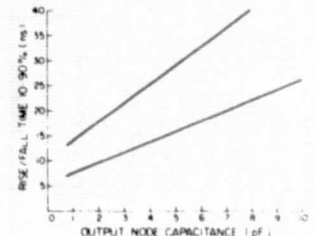
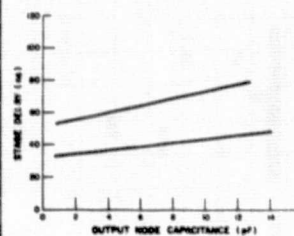
$$X = A \oplus B$$

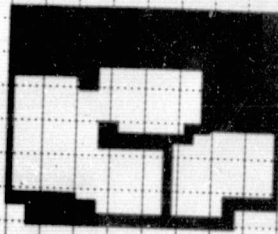
TRUTH TABLE

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

CELL I/O CAPACITANCE VALUES

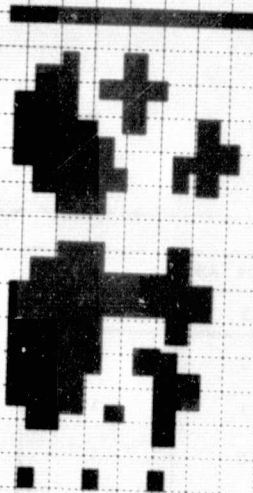
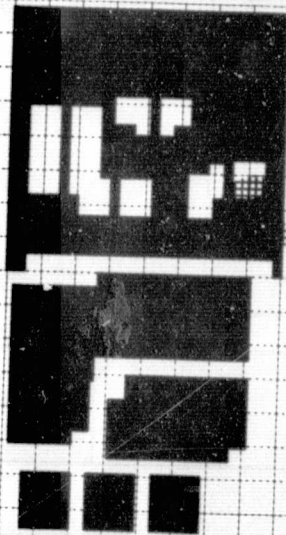
PIN	CAPACITANCE (pF)
2	1.03
3	1.69
4	2.22





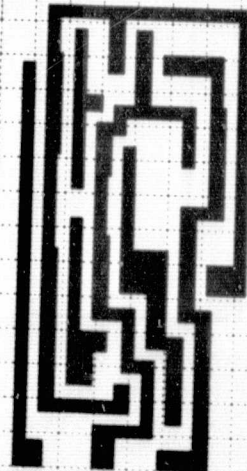
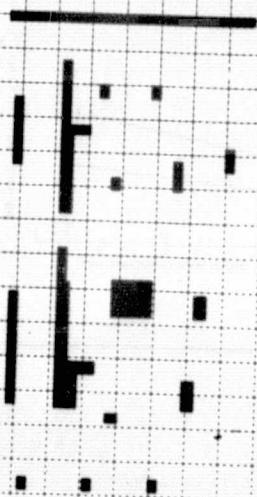
LEV 1

LEV 2



LEV 3

LEV 4



LEV 5

LEV 6

ORIGINAL PAGE IS
OF POOR QUALITY

TOP/BOTTOM DUMMY PAD

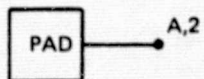
C-MOS STANDARD
CELL NO. 9000

0 Devices

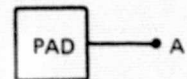
1 Pad

Cell Width = 8.0 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

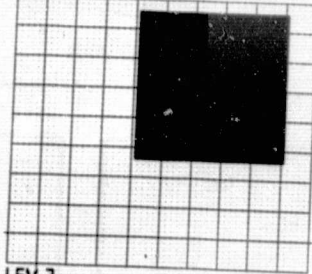
TRUTH TABLE

A	
N/A	N/A

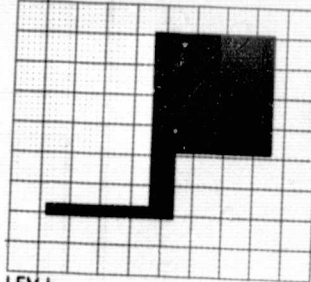
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.38

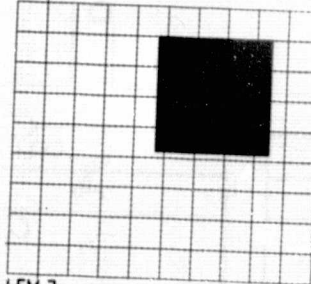
MSFC C 9000



LEV 3



LEV b



LEV 7

ORIGINAL PAGE IS
OF POOR QUALITY

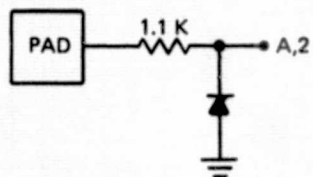
SIDE INPUT PAD

Devices Resistor-Diode Protection
Pad 1

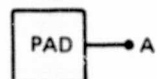
Cell Width = 8.0 mils

C-MOS STANDARD
CELL NO. 9010

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

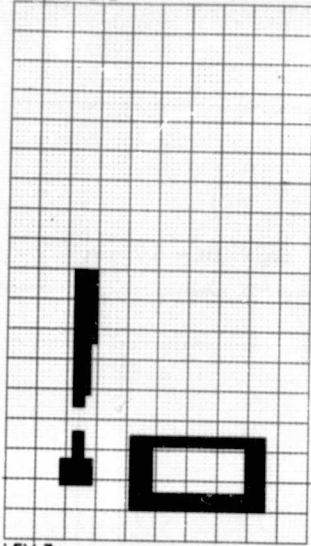
TRUTH TABLE

A	
N/A	N/A

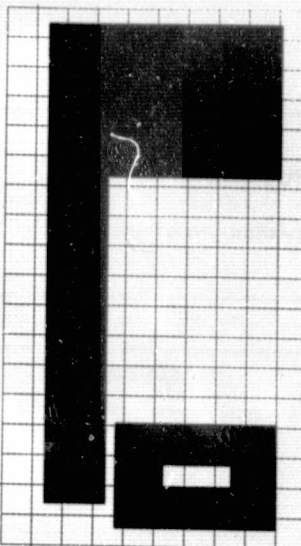
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.2

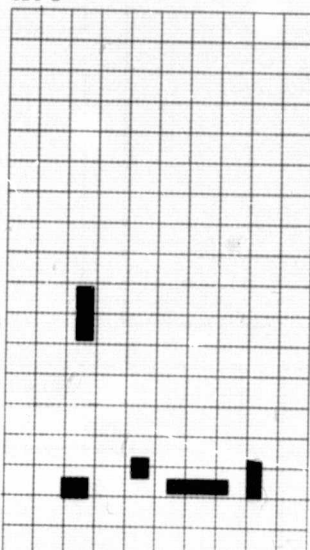
MSFC C 9010



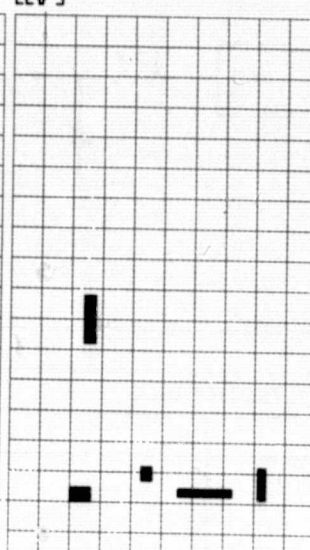
LEV 2



LEV 3

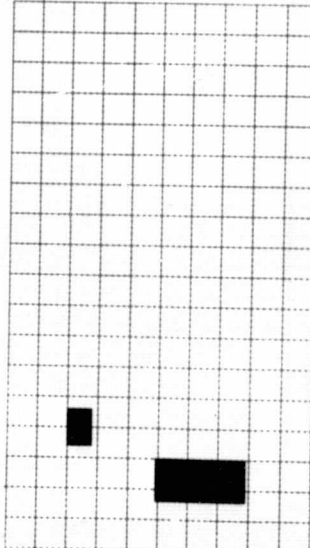


LEV 4

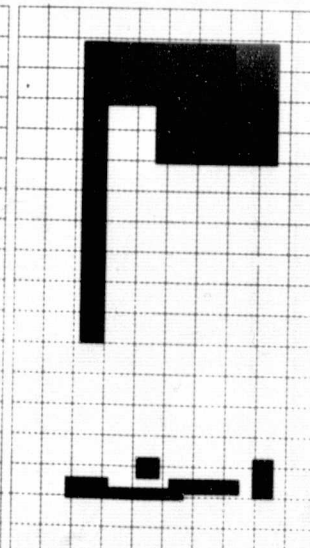


LEV 5

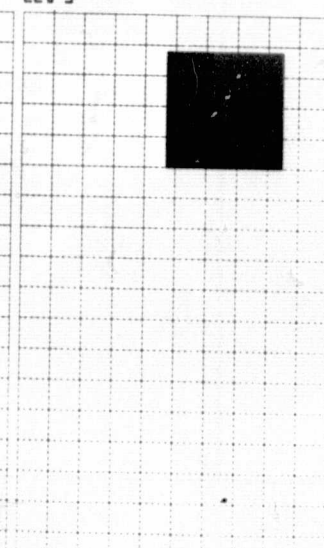
MSFC C 9010



LEV 1



LEV 6



LEV 7

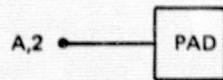
TOP/BOTTOM OUTPUT PAD

0 Devices
1 Pad

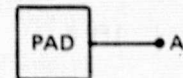
Cell Width = 8.0 mils

C-MOS STANDARD
CELL NO. 9020

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

TRUTH TABLE

A	
N/A	N/A

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.92

MSFC C 9020

LEV 2

LEV 3

LEV 4

LEV 5

LEV 6

LEV 7

ORIGINAL PAGE IS
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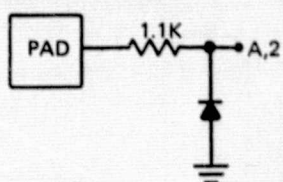
TOP/BOTTOM INPUT PAD

Devices Resistor-Diode Protection
Pad 1

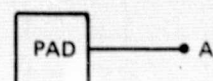
Cell Width = 8.0 mils

C-MOS STANDARD
CELL NO. 9030

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

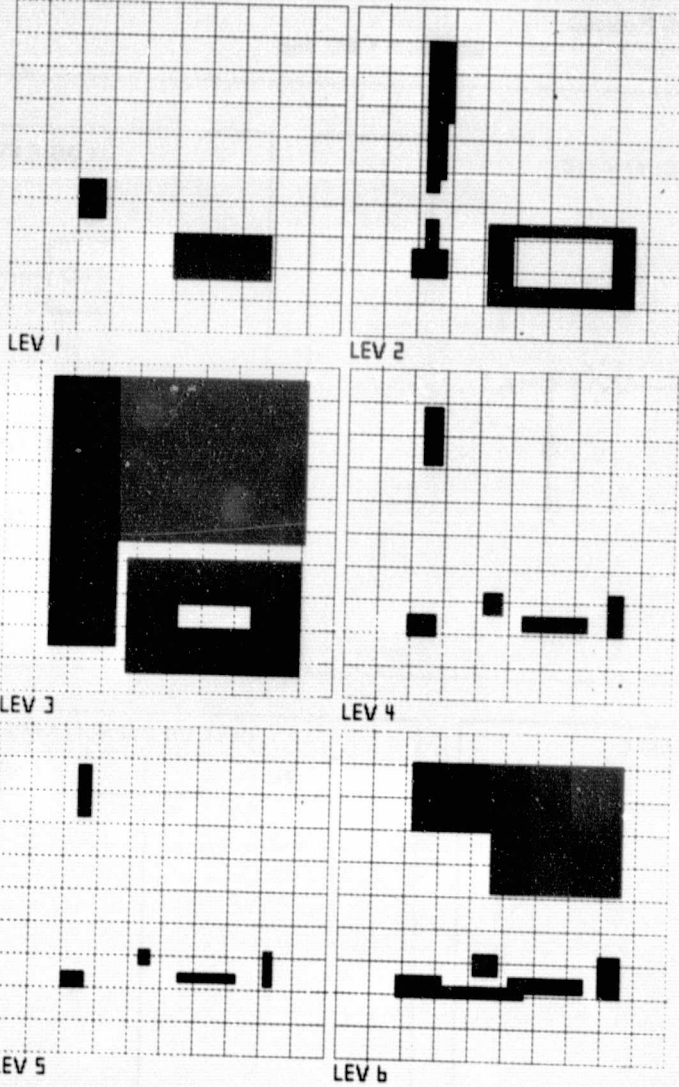
TRUTH TABLE

A	
N/A	N/A

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.06

MSFC C 9030



ORIGINAL PAGE IS
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TOP/BOTTOM PAD WITH PULL UP RESISTOR

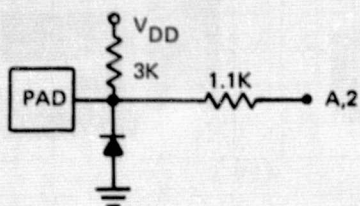
C-MOS STANDARD
CELL NO. 9040

Devices Pull Up Resistor, Resistor-Diode Protection

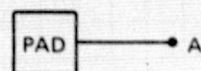
1 Pad

Cell Width = 8.0 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

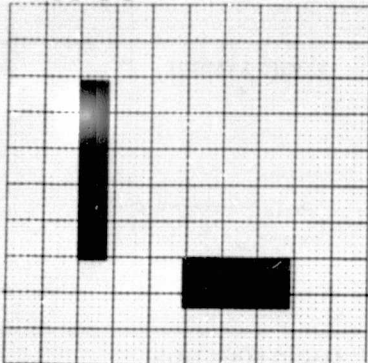
TRUTH TABLE

A	
N/A	N/A

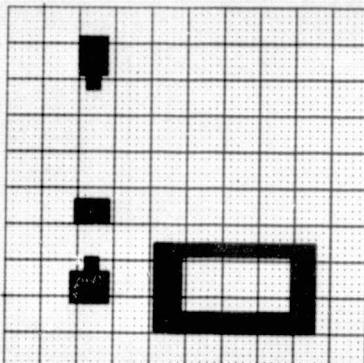
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.9

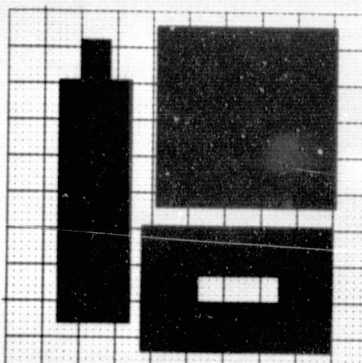
MSFC C 9040



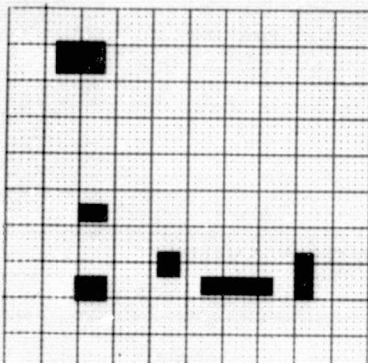
LEV 1



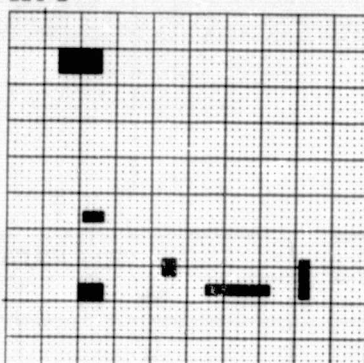
LEV 2



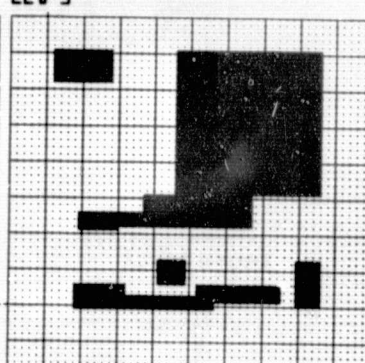
LEV 3



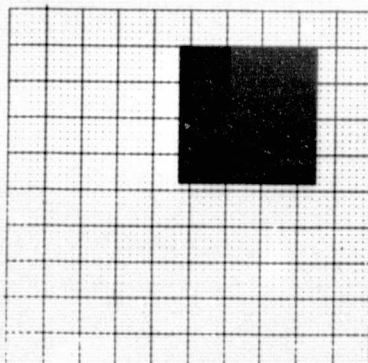
LEV 4



LEV 5



LEV 6



LEV 7

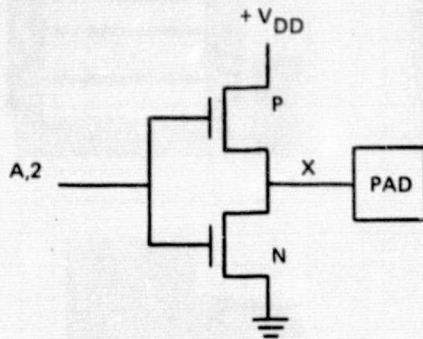
SIDE PAD WITH DRIVER INVERTER

C-MOS STANDARD
CELL NO. 9050

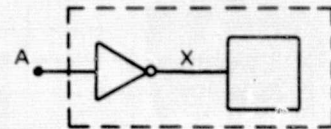
2 Devices
1 Pad

Cell Width = 10.0 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

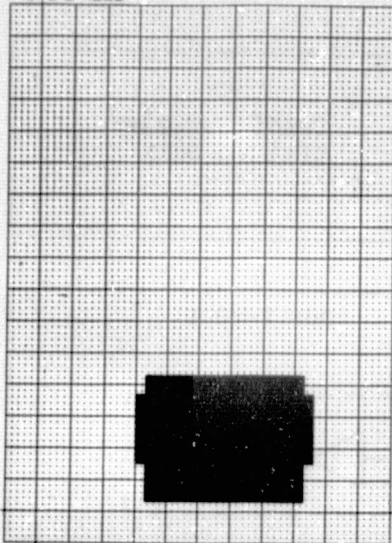
$$X = \bar{A}$$

TRUTH TABLE

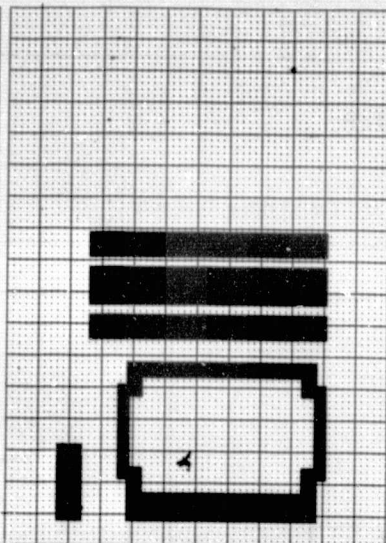
A	X
0	1
1	0

CELL I/O CAPACITANCE VALUES

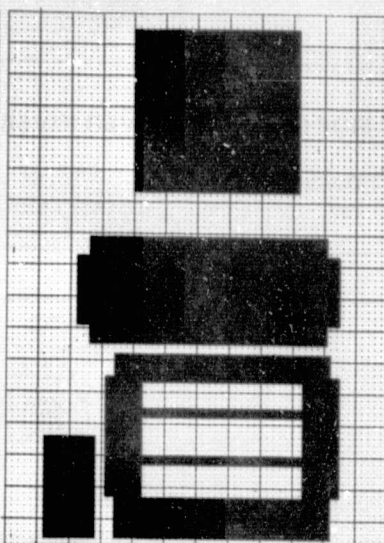
PIN	CAPACITANCE (pF)
2	2.9
X	1.6



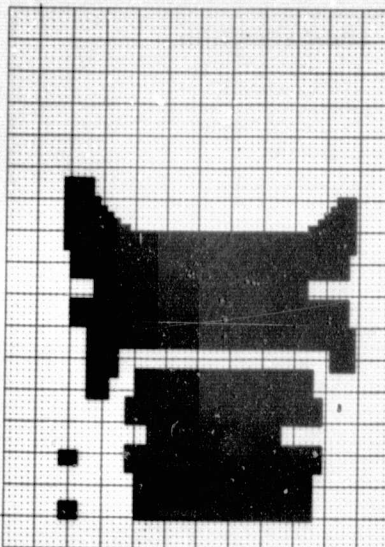
LEV 1



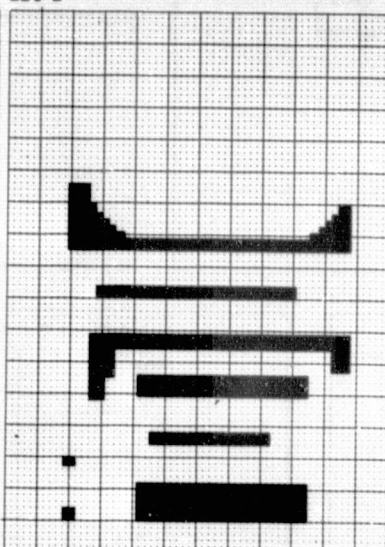
LEV 2



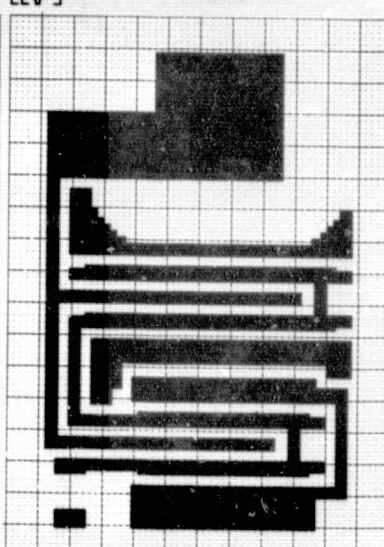
LEV 3



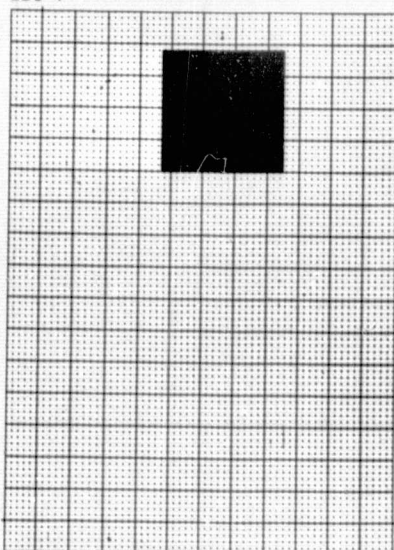
LEV 4



LEV 5



LEV 6



LEV 7

ORIGINAL PAGE IS
OF POOR QUALITY

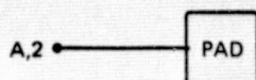
SIDE OUTPUT PAD

0 Devices
1 Pad

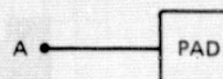
**C-MOS STANDARD
CELL NO. 9070**

Cell Width = 8.0 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

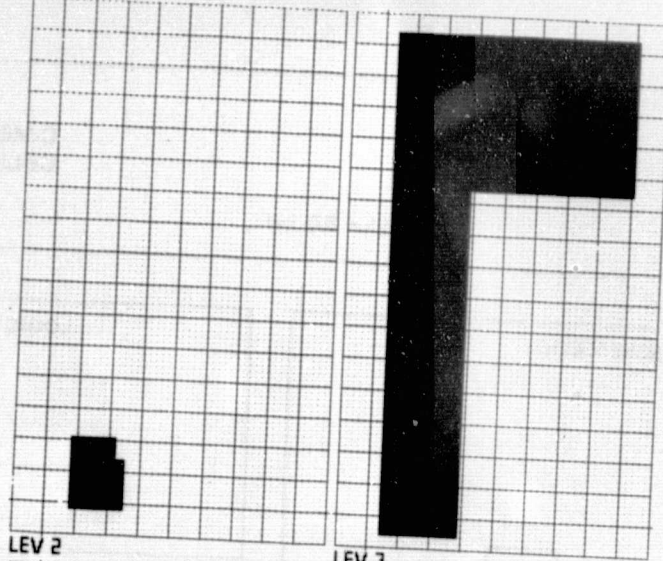
TRUTH TABLE

A	
N/A	N/A

CELL I/O CAPACITANCE VALUES

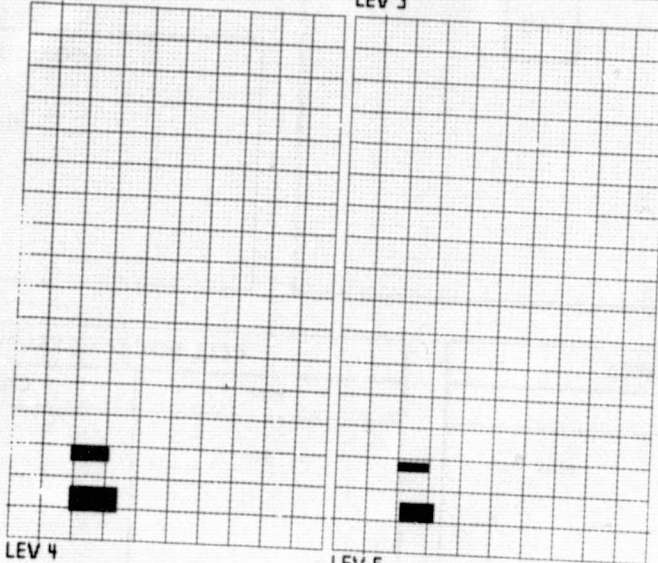
PIN	CAPACITANCE (pF)
2	0.92

MSFC C 9070



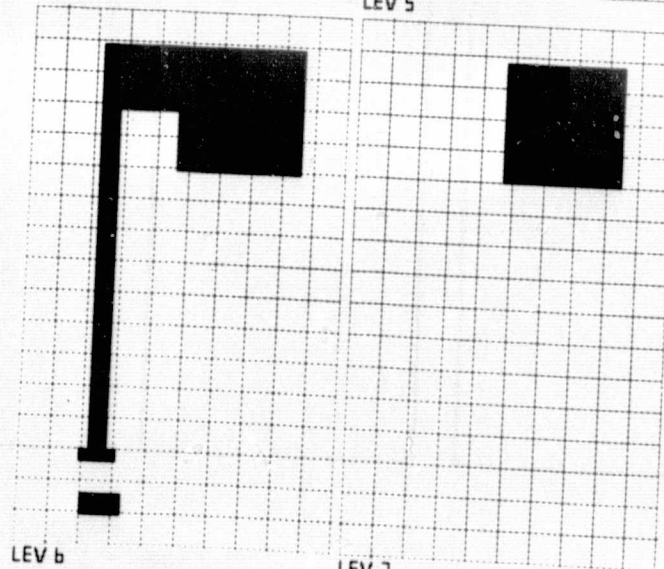
LEV 2

LEV 3



LEV 4

LEV 5



LEV 6

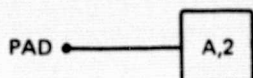
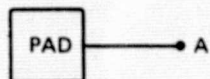
LEV 7

SIDE DUMMY PAD

0 Devices
1 Pad

Cell Width = 8.0 mils

C-MOS STANDARD
CELL NO. 9080

SCHEMATIC**LOGIC SYMBOL****LOGIC EQUATION**

N/A

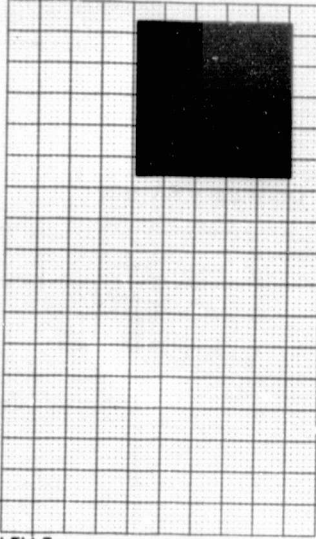
TRUTH TABLE

A	
N/A	N/A

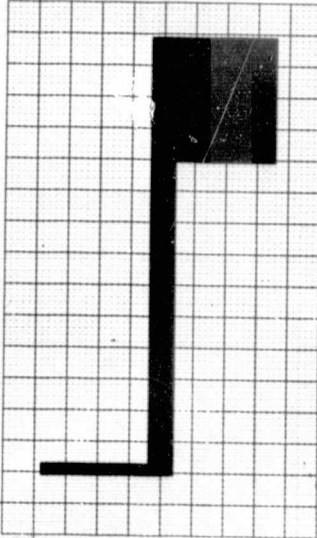
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	0.37

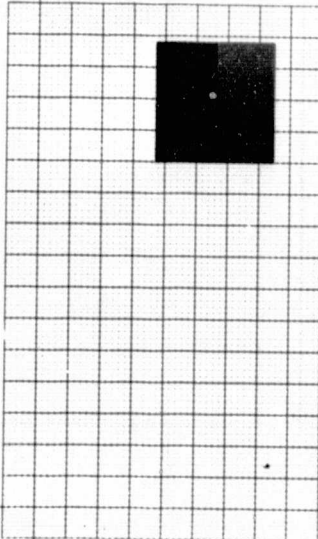
MSFC C 9080



LEV 3



LEV b



LEV 1

ORIGINAL PAGE IS
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GROUND PAD

0 Devices

1 Pad

Cell Width = 6.0 mils

**C-MOS STANDARD
CELL NO. 9100****SCHEMATIC**

PAD

LOGIC SYMBOL

PAD

LOGIC EQUATION

N/A

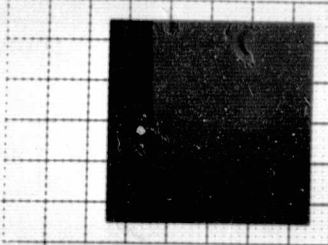
TRUTH TABLE

A	X
N/A	N/A

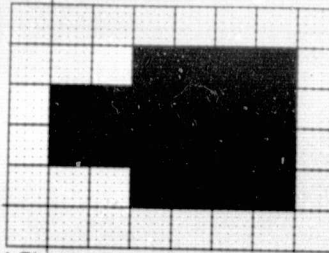
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

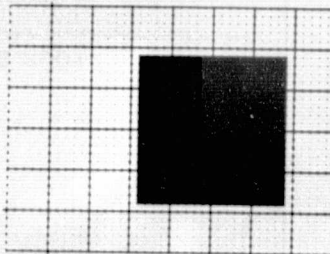
MSFC C 9100



LEV 3



LEV 6



LEV 7

ORIGINAL PAGE IS
OF POOR QUALITY

V_{DD} PAD

0 Devices

1 Pad

C-MOS STANDARD
CELL NO. 9110

Cell Width = 6.0 mils

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

N/A

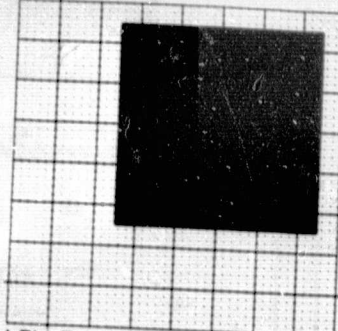
TRUTH TABLE

A	X
N/A	N/A

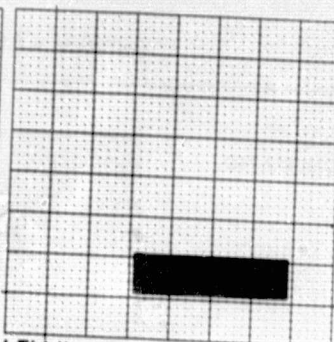
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

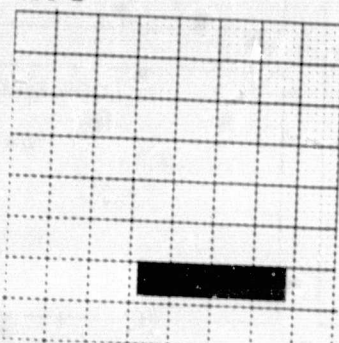
MSFC C 9110



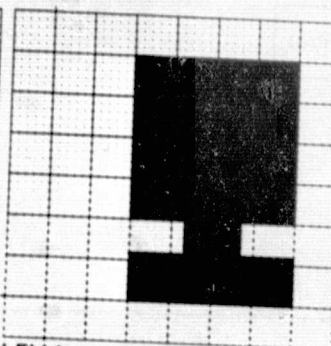
LEV 3



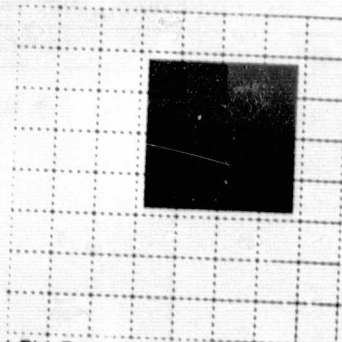
LEV 4



LEV 5



LEV 6



LEV 7

ORIGINAL PAGE IS
OF POOR QUALITY

LONG GROUND PAD

0 Devices
1 Pad

Cell Width = 13.8 mils

C-MOS STANDARD
CELL NO. 9120

SCHEMATIC

PAD

LOGIC SYMBOL

PAD

LOGIC EQUATION

N/A

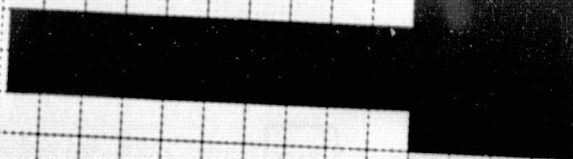
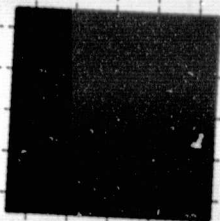
TRUTH TABLE

A	X
N/A	N/A

CELL I/O CAPACITANCE VALUES

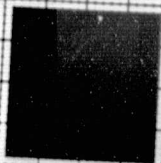
PIN	CAPACITANCE (pF)
N/A	N/A

MSFC C 9120



LEV 3

LEV 6



LEV 7

ORIGINAL PAGE IS
OF POOR QUALITY

OFF-CHIP ALIGNMENT MARKS**C-MOS STANDARD
CELL NO. 9210, 9220
9230, 9240, 9250, 9260****SCHEMATIC**

N/A

LOGIC SYMBOL

N/A

LOGIC EQUATION

N/A

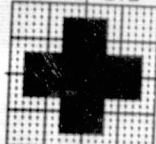
TRUTH TABLE

A	X
N/A	N/A

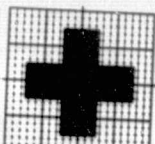
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

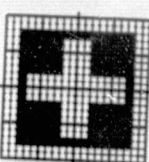
MSFC C 9210



LEV 1



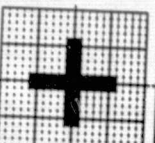
LEV 2



LEV 3



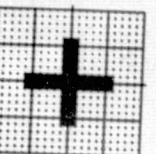
LEV 4



LEV 5



LEV 6

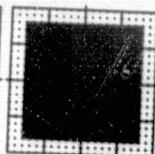


LEV 7

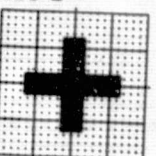
MSFC C 9220



LEV 3

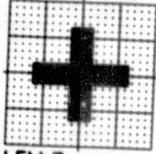


LEV 4

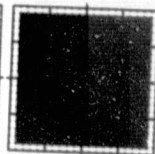


LEV 6

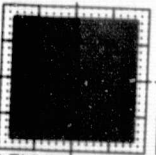
MSFC C 9230



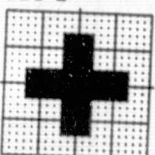
LEV 2



LEV 3

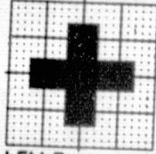


LEV 4

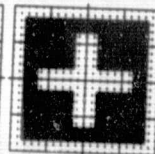


LEV 6

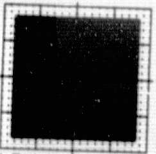
MSFC C 9240



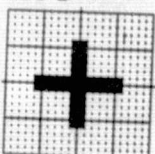
LEV 2



LEV 3

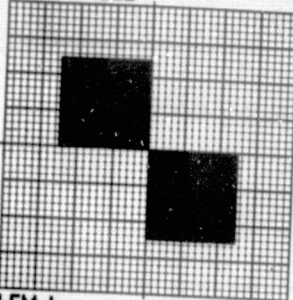


LEV 4

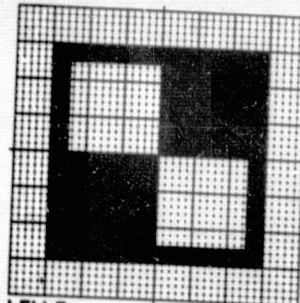


LEV 5

MSFC C 9250

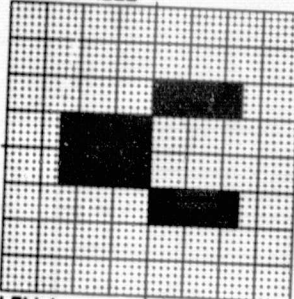


LEV 1

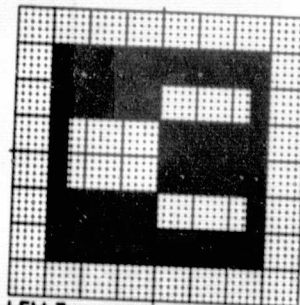


LEV 3

MSFC C 9260



LEV 1



LEV 3

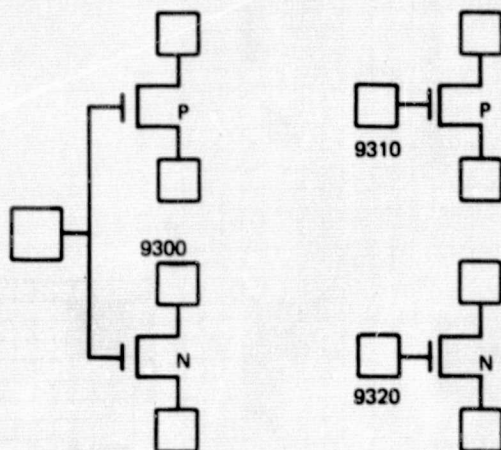
ORIGINAL PAGE IS
OF POOR QUALITY

9300 – P AND N TEST TRANSISTORS
 9310 – P – TEST TRANSISTOR
 9320 – N – TEST TRANSISTOR

DISCRETE DEVICES

C-MOS STANDARD
 CELL NO. 9300,
 9310, 9320

SCHEMATIC



LOGIC SYMBOL

N/A

LOGIC EQUATION

N/A

TRUTH TABLE

A	X
N/A	N/A

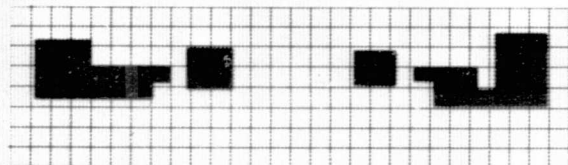
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

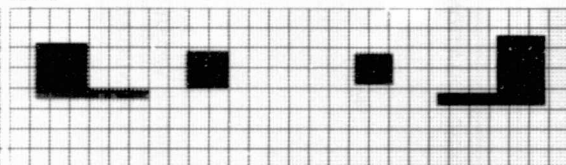
MSFC C 9300



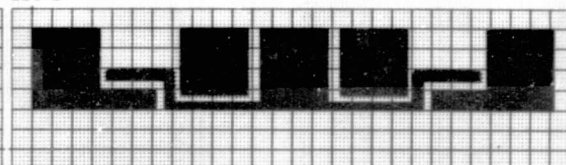
LEV 1



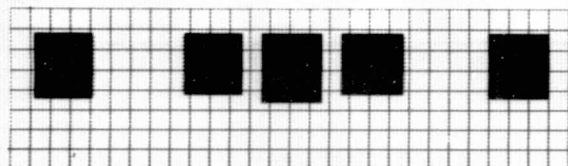
LEV 2



LEV 3



LEV 4



LEV 5

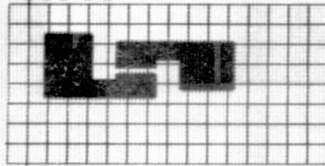


LEV 6

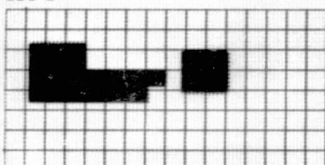


LEV 7

MSFC C 9310



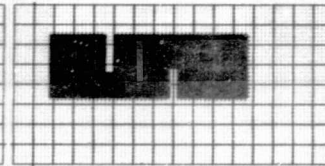
LEV 2



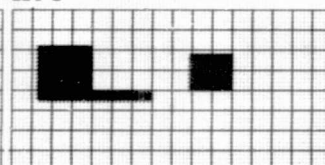
LEV 4



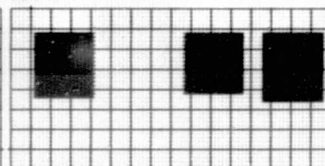
LEV 6



LEV 3

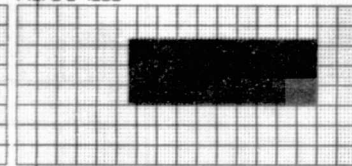


LEV 5

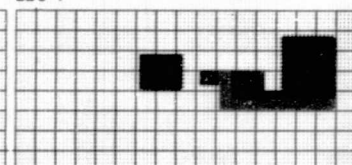


LEV 7

MSFC C 9320



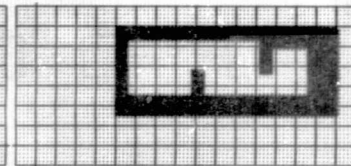
LEV 1



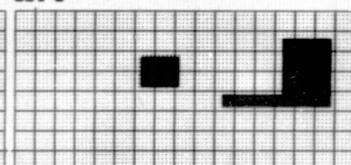
LEV 4



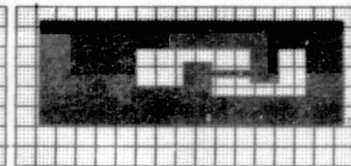
LEV 7



LEV 2



LEV 5



LEV 3



LEV 6



IDENTIFICATION CELLS

*9430 — Level 6 only of 9420

C-MOS STANDARD
CELL NO. 9400,
9410, 9420, 9430,*
9440, 9450

SCHEMATIC

N/A

LOGIC SYMBOL

N/A

LOGIC EQUATION

N/A

TRUTH TABLE

A	X
N/A	N/A

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

MSFC C 9400

LEV 1 LEV 2 LEV 3

LEV 1

LEV 2

LEV 3

LEV 4 LEV 5 LEV 6

LEV 4

LEV 5

LEV 6

LEV 7

LEV 7

MSFC C 9410

NASAC

LEV 1

MSFC C 9420

MSFC C

LEV 1

MSFC C 9440

C

LEV 6

MSFC C 9450

MSFC

LEV 6

9500 – FEEDTHROUGH TO P+ DIFFUSION
 9510 – FEEDTHROUGH TO N+ DIFFUSION
 9600 – CELL ROW END CAP

C-MOS STANDARD
 CELL NO. 9500, 9510
 9600

SCHEMATIC

N/A

LOGIC SYMBOL

N/A

LOGIC EQUATION

N/A

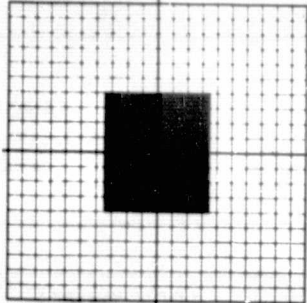
TRUTH TABLE

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N/A	N/A

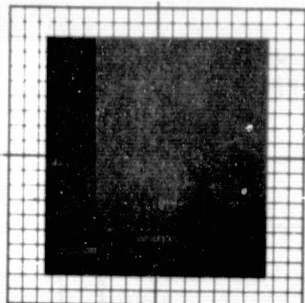
CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
N/A	N/A

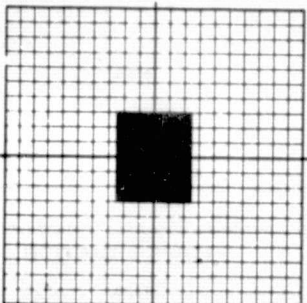
MSFC C 9500



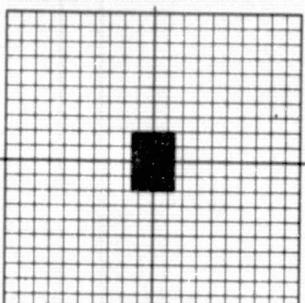
LEV 2



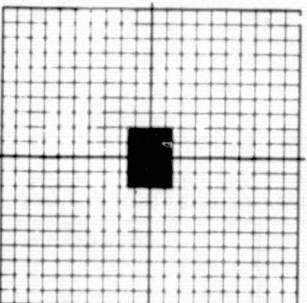
LEV 3



LEV 4

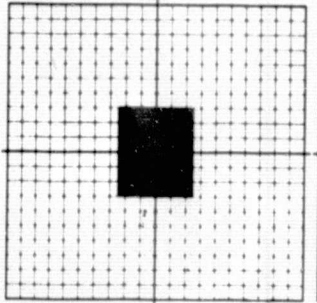


LEV 5

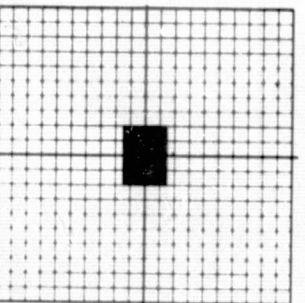


LEV 6

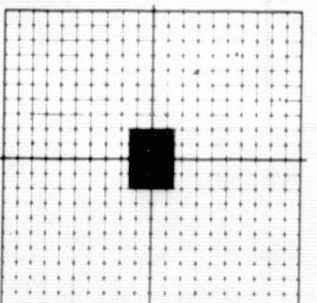
MSFC C 9510



LEV 4

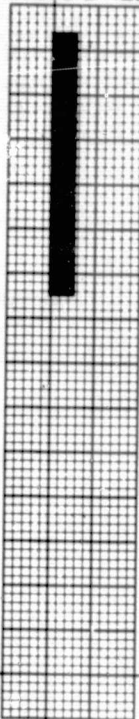


LEV 5

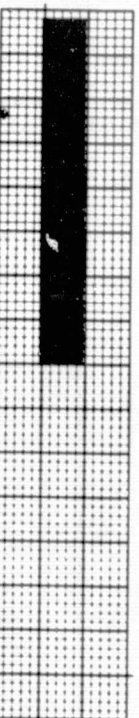


LEV 6

MSFC C 9600



LEV 2



LEV 3

9700-9790 NUMERIC CHARACTERS 0-9 (ALL LEVELS)
 9800-9890 NUMERIC CHARACTERS 0-9 (LEVEL 6 ONLY)

9800-9890 ARE NOT PICTURED
 USE 9700-9790 FOR REFERENCE

C-MOS STANDARD
 CELL NO.
 9700 TO 9790
 9800 TO 9890

SCHEMATIC

N/A

LOGIC SYMBOL

N/A

LOGIC EQUATION

N/A

TRUTH TABLE

A	X
N/A	N/A

CELL I/O CAPACITANCE VALUES

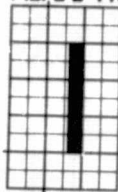
PIN	CAPACITANCE (pF)
N/A	N/A

MSFC C 9700



LEV I

MSFC C 9710



LEV I

MSFC C 9720



LEV I

MSFC C 9730



LEV I

MSFC C 9740



LEV I

MSFC C 9750



LEV I

MSFC C 9760



LEV I

MSFC C 9770



LEV I

MSFC C 9780



LEV I

MSFC C 9790



LEV I